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Prevention of Single Event Upsets in Microelectronics

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13. ABSTRACT *(Maximum 200 words)*

Experimental and analytical studies of basic single-event radiation effects, single-event upset (SEU) modelling, and single-event upset hardening were performed. The effects of total-dose and proton environments on SEU responses are presented and quantified. Improved modelling and hardening techniques for SEU and GaAs and bipolar SRAMs are also presented. Techniques for SEU reduction in circuits, including a novel decoupling resistor structure, were evaluated.

*Part of this work was conducted at Vanderbilt University.

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CMOS	Proton	

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PREFACE

The efforts reported on in this document, covering several research areas and a period of four years, have benefitted considerably from the assistance of many people. Unfortunately, the following list is bound to be incomplete. Nevertheless, the authors of this report would like to acknowledge their appreciation to the Circuit Simulation Group at North Carolina State University, and especially to George Hatem and the graduate students in the group who contributed to removing numerous "hitches in our get-along" during the course of this research, and to the Space Electronics Research Group at Vanderbilt for similar heroic contributions.

Our colleagues in the radiation hardened IC community have stimulated and contributed many "seeds" for ideas grown throughout this effort. We are especially grateful to our colleagues at the Naval Research Laboratory, especially Art Campbell and Bill Stapor, at Texas Instruments, Inc., especially Ted Houston, Larry Hite, and Gordon Pollack, at Harris Semiconductor, especially Jeff Lee, Tom Haycock, and Ken Jones, and at Mission Research Corporation, especially Dave Alexander, Ron Pease and Dave Mavis for many helpful discussions and for providing device data and test results.

We are thankful to our "PARs", Ed Petersen and Harvey Eisen for their patient and capable guidance, and to our sponsors for providing us the opportunity to learn things from research efforts they funded which have contributed to our work on the projects reported herein.

Finally, we are grateful to our universities, North Carolina State and Vanderbilt, for providing their considerable support. Special thanks is due the Vanderbilt Department of Electrical Engineering for supporting graduate students who have contributed very considerably to the work reported here.

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SECTION 1

INTRODUCTION

This document provides a report on four years of research. The contract under which the work has been performed was with North Carolina State University (NCSU). The first year's efforts, conducted at NCSU, considered single-event effects on silicon and gallium arsenide integrated circuits. The mechanisms for upset and methods to harden circuits against single-event upset were studied. During the second, third and fourth years, Vanderbilt University held a subcontract for silicon studies, and NCSU continued research on gallium arsenide ICs. The Vanderbilt research comprised two main areas: the development of a software tool, PARA, for analysis of the chip level response of digital CMOS ICs to total dose radiation, including identification of failure modes and levels, and single-event upset analyses of CMOS-SOI devices and circuits, including identification, description and parameterization of the event amplification due to the effects of the parasitic bipolar device inherent within CMOS-SOI transistors. A third, smaller research topic at Vanderbilt has been an investigation of the effect of digital logic scaling on single-event vulnerability.

This report is organized by research subject area into five technical sections. The first three cover the Vanderbilt research products and the fourth and fifth the NCSU research products. A final section provides an overview of conclusions. Each section is written to "stand alone"; this is intended to allow readers who are interested in only one of the projects to most easily benefit from this report.

Appendices at the end of this document provide additional information on PARA. The section of this report describes our PARA research underway on PARA extensions. PARA is designed to be a modular simulation tool, and to easily accept additional modules extending its applicability to non-CMOS technologies and to the study of additional failure mechanisms. Extensions of PARA have not been directly funded by this contract, but have been supported by Vanderbilt University. Nevertheless, the work reported here has greatly benefitted from the products of research under this contract, and should be of interest to the community reading this report. For these reasons, these appendices have been provided.

The software tools and techniques developed under this contract, and described in this report are public domain. Present research efforts are underway to provide independent and comprehensive verification of the accuracy of these tools, to enhance their user interfaces, to document their use by those interested in IC vulnerability and reliability analyses (even if they are unfamiliar with the details of computer analysis tools), and to distribute these tools and techniques to the larger community interested in radiation effects on ICs. It is anticipated that these efforts will be complete within the next year, at least for the more mature portions of software covered in the main text. Software copies for general distribution should be available in 1991; copies for "alpha" siting, i.e., for evaluation, can be obtained by contacting the authors of this report.

Several appendices appear at the end of this report. They describe research projects which were investigated at Vanderbilt University during 1987-1990. Appendix A is the user's manual for PARA. Appendix B describes the topology-dependent failure-exposure levels for CMOS ICs and radiation hardening techniques at the logic level. Appendix C describes a software program under development, PARASTAT, for statistical analysis of radiation effects and failure mechanisms. Appendix D describes a new software of PARA, TODO, which is capable of identifying the failure mechanisms for bipolar, NMOS, and CMOS circuits. Appendix E describes a circuit simulator capable of simulating transient radiation effects on CMOS combinational circuits.

Currently, we are working on PARASTAT and TODO to improve the simulation algorithms and efficiency. A new user interface is also being developed which will combine all these software packages into one universal package. We are also developing software for automatic test vector generation based on the worst-case bias conditions identified by PARA. In addition, we are in the process of developing software capable of estimating the SEU vulnerability of a combinational circuit.

SECTION 2

THE PARA PROJECT

2.1 INTRODUCTION.

Advances in semiconductor technology in the last few years greatly increased the complexity and the packaging density of Integrated Circuits (ICs). This increase in the number of the devices has also brought a decrease in device costs, along with improved performance. However, a problem never adequately solved for ICs is still with us and is getting much worse: the problem of testing, or determining in a cost effective way whether an IC has been manufactured correctly. With increased complexity of Very Large Scale Integrated (VLSI) circuits, simulation/testing has proved to be an almost impossible task and manufacturers looked for better ways to assure the reliability of parts.

With the advent of fast computers and developments in numerical methods, computer aided simulation/testing has proved to be the best approach. Many simulation programs have been developed for Computer-Aided Design (CAD) and testing of ICs. However, CAD tools currently available for simulation and testing are rapidly becoming obsolete because of inefficient algorithms which require longer time periods for simulation of (VLSI) circuits [1-3]. This has created a need for faster and more efficient simulators. New special-purpose simulators have been developed which trade off accuracy for speed to replace conventional, general purpose simulators [4]. These special-purpose simulators are suitable only for specific types of simulations for a particular technology and operating environment. However, by trading off generality and using available information about the technology and operating environments, a simulator can be made more efficient by reducing simulation problems to a smaller subset of the analysis of critical conditions. One area of circuit simulation which falls in the above category is the circuit simulation of radiation effects. Usually, very high reliability is required of the parts bound for radiation environments. Hence, these parts must be simulated and tested thoroughly to achieve the required confidence level. The problems created by the radiation exposure of integrated circuits are unique and so unusual that thorough simulation and testing of VLSI circuits is extremely difficult and new ways to estimate the operating performance of a circuit in a radiation environment must be developed. This requires innovative simulation and modeling techniques. The work reported here presents a new simulator, PARA, to aid the circuit simulation and testing of radiation effects.

PARA is specifically developed for Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) technology. CMOS technology is best suited for radiation environments due to high noise immunity, low power requirements, and higher packing density [5]. Other technologies, such as bipolar technology and gallium arsenide (GaAs) technology, will be considered in the future versions of the software.

For CMOS technology, the electrical characteristics of devices, when exposed to ionizing radiation, change so as to degrade their performance [6]. These degradations in device characteristics decrease the circuit performance and may cause circuit failure after long-term exposure [7]. For Metal Oxide Semiconductor (MOS) technology, these device parameter shifts are a strong function of the operating voltages of devices during irradiations [8]. As the improper function of even a single device may constitute failure for the whole IC, each device must be tested individually to insure identifying the earliest circuit failure due to radiation exposure. Due to the bias dependency associated with the operating performance of a device, all possible combinations of operating voltages for each device must be checked to verify functionality after radiation exposure. These bias-dependent device parameter shifts make identification of failure mechanisms and test vectors to induce these failure mechanisms a highly complex process for VLSI circuits. Using conventional simulation techniques, testing and simulation time requirements increase exponentially with the number of devices comprising the IC. The new simulation methodology presented here, and implemented in PARA, alleviates the above mentioned problem areas and provides faster and more efficient circuit simulation of CMOS VLSI circuits.

PARA considers the failure mechanisms and their associated operating conditions for VLSI circuits exposed to radiation environments. These failure mechanisms were previously not understood or simulated by computer because of difficulties involved in using conventional simulators. The goal of this research was to identify possible failure mechanisms and the associated operating conditions for a CMOS circuit operating in a radiation environment and to propose new algorithms for effective simulation. The identification of failure mechanisms can greatly enhance the circuit designer's capability to optimize the operating life of a circuit design. Also, by specifying the operating conditions causing earliest operational failure, the simulator significantly reduces the testing time for VLSI designs.

2.2 FAILURE MECHANISMS.

This section reviews failure mechanisms and failure modes possible for CMOS integrated circuits operating in radiation environments. The dependence of these mechanisms on operating voltages during and after irradiation is discussed. The identification of these failure mechanisms makes the process of redesigning circuits more efficient and faster. Also, the identification of worst-case operating conditions to induce these failures can be used to generate test vectors for critical testing. Current methodologies for simulation and testing of VLSI circuits are also reviewed to emphasize the need for faster and efficient simulation algorithms.

2.2.1 Failure Modes.

The primary total-dose effects for MOS devices are a shift in threshold voltage, decreased mobility, and increased leakage currents [6]. For n-channel devices, a negative threshold voltage shift will increase the ON-state drive current, and, more importantly, increase the OFF-state

leakage current. For p-channel devices, a negative threshold voltage shift will reduce the ON-state drive current. Carrier mobility degradation will occur for both types of devices. A positive threshold voltage shift in n-channel devices, the "rebound" process [11], decreases the ON state drive current. Therefore, total-dose induced circuit failures are assumed to either involve excess leakage currents in n-channel devices and insufficient drive in p-channel devices or insufficient drive for p-channel and n-channel devices along with decreased carrier mobilities. During irradiation, resulting threshold voltage shift magnitudes are largest for n-channel devices which are biased ON and for p-channel devices which are biased OFF. Keeping these effects in mind, radiation-induced failure mechanisms can be classified into three categories: power supply-related failures, static failures, and dynamic failures [7, 9, 10]. The identification of these failure mechanisms enables the circuit designer to extract the operating conditions which will cause the desired device parameter degradations to the critical devices in a circuit.

Power supply-related failures will occur if chip-wide leakage through n-channel devices exceeds the maximum allowable supply current. Usually, the maximum supply current is determined by system-level constraints on power allocation rather than by device functionality. The failure is to be interpreted here as exceeding the operating specifications of the power supply manufacturer. The excessive operating current may overload the power supply and may also cause heat dissipation problems. In extreme cases, electro-migration and rail span collapse may also occur. Such failures are gradual failures, meaning that slow degradations in device parameters will increase the current slowly until the failure level is reached. The circuit and the power supply must be monitored constantly to identify such failures. The standby leakage current increases exponentially with dose. At higher total-dose exposures, the heat dissipation problems may cause the circuit performance to degrade. The ICs reviewed in this report ceased to operate normally at about 50 kRads(Si) total-dose expcsure.

Static failures occur if leakage currents of n-channel devices coupled with reduced current drive for p-channel devices prevent the signal at a critical node from reaching a valid HIGH logic level. This type of failure will occur at the lowest dose in poorly-ratioed static logic gates. Poorly-ratioed gates here indicates unequal rise and fall time for the gate. The CMOS NOR gate of Figure 1 provides an example of a circuit that is highly prone to static failure. If the n-channel devices are biased ON during irradiation and the p-channel devices are biased OFF, and if after irradiation a HIGH logic-level output is desired, the combined effect of total-dose-induced shifts may result in a weak or undefined output. This error will be magnified if the following stage has experienced precisely the opposite irradiation biases. For example, if the following stage is an inverter, the worst case will occur for an irradiation bias with the n-channel device OFF and the p-channel device ON, since this will cause the inverter to have the highest possible post-radiation logic threshold. The potential for static failures at a given node can be quantified using a simple ratio of the n-channel to p-channel conductance paths, and worst-case irradiation parameters can be assigned as in the example.

Dynamic failures will occur for signal paths from an input node to an output node where the reduced current drive of p-channel devices, increased leakage of n-channel devices, and decreased mobilities of holes and electrons lead to increased delay for input signal transitions. The added

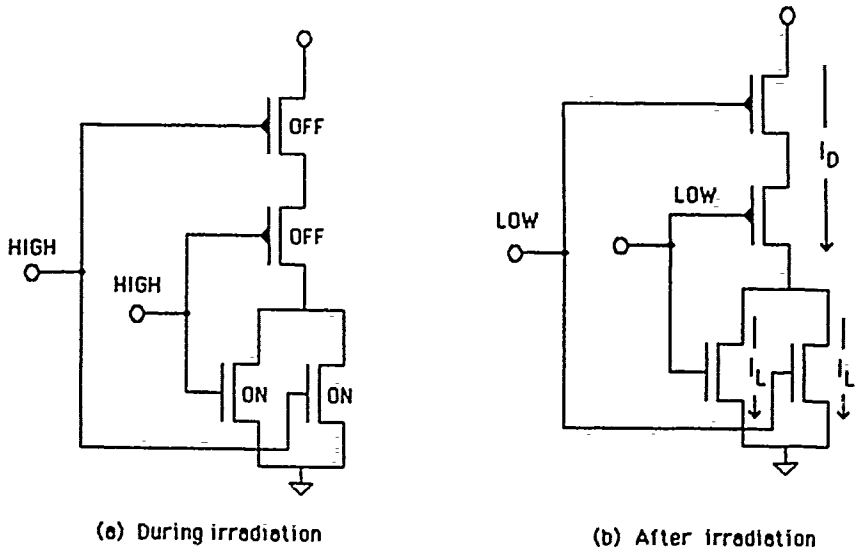


Figure 1. A CMOS NOR gate with worst-case bias conditions.

delay introduced by these device parameter degradations can result in failure of synchronous circuit operation along the signal path. Referring to Figure 1, assume that the n-channel devices of NOR gate are biased ON during irradiation and the p-channel devices are biased OFF. This will induce maximum device parameter shifts for these devices, i.e. p-channel will have least current driving capability and n-channel will have maximum leakage current. For the next stage, ON p-channel and OFF n-channel device during irradiation will induce higher threshold voltage for n-channel devices and lower threshold voltage for p-channel devices. This pattern of device parameter shifts is repeated until the signal path terminates. After irradiation, if the inputs of this NOR gate switch from HIGH-to-LOW, the delay for the gate is higher than the delay caused by any other input vector for NOR gate. This is because of the fact that HIGH-to-LOW transition at the inputs of NOR gate will face higher threshold voltages for p-channel devices and increased leakage of n-channel devices. For any other transition at the input, one of the n-channel devices will be turned ON. The increased current sinking capability of these devices due to decreased threshold voltage actually decreases the delay through the gate. Thus, for one transition at the inputs, the gate will offer higher delay for the signals passing through, and for other transitions, the gate will offer lower delay for signals. This indicates that like static failures, dynamic failures are operating-bias dependent. For one combination of input conditions during and after irradiation, the circuit may function properly but it may fail for another combination.

Additional failure mechanisms can be similarly identified for the case of rebound. Rebound, which can occur for a large total-dose exposure, is a condition where the n-channel threshold voltage increases and eventually exceeds the pre-radiation threshold voltage. The rebound failure mechanism will involve circuit operating conditions where diminished current-driving capability

of both n- and p-channel devices leads to failure. Failures due to rebound are a subset of dynamic failures. Rules for identifying sensitive nodes for the rebound failure mechanisms can be constructed in a similar manner as the rules described above for dynamic failures. Worst-case irradiation parameters can be also defined in a consistent manner.

It is evident from the above discussion that to completely assure proper operation of the circuit operation in a total-dose environment, one must expose the circuit to total dose for every possible combination of input vectors during and after irradiation to identify the worst-case combination of operating conditions: an impossible task for VLSI circuits. Thus, radiation hardening and survivability issues can only be thoroughly evaluated by combining computer simulation and testing strategies. The task of simulating a VLSI circuit using conventional simulators is a highly complex one due to the large number of transistors involved [4]. The problem of exhaustively testing integrated circuits is also complex and is becoming more so because of increasing packing density of IC's [12]. These problems can be easily solved by using innovative and highly efficient methodologies for testing and simulation. Computer simulators can be used to identify the critical test conditions and testing can be used to actually verify the circuit's performance under critical test conditions.

2.2.2 Testing and Simulation.

There are many techniques available to reduce the complex problem of testing an IC into a manageable problem [4, 12, 13]. These testing methodologies comprise of techniques for self testing, or design for testability. These techniques are divided into two categories. The first category is the Ad Hoc techniques and the second is the structured approach. The Ad Hoc techniques are applicable only to a certain set of designs, not to all designs. The structured techniques are applicable for all designs and usually involve a set of design rules by which designs are implemented. The objective of the approach reported here is to reduce the sequential complexity of a network to aid test generation and fault detection.

In the Ad Hoc category, the first technique is partitioning. Partitioning refers to disconnecting one portion of a network from another in order to make testing easier. This approach is impossible for ICs. Another approach is to add extra probing sites at the critical points in the circuit. This approach is also unsuitable for VLSI circuits due to routing requirements, pad size, and the number of pads required for a complete analysis. Another approach is to use signature analysis. Any output of a digital circuit will follow a fixed pattern for a fixed input pattern. Any deviation from this fixed pattern at the output indicates a circuit failure.

For all these approaches, only failure detection is possible. No information is obtained about the failure mechanism, or how to improve the circuit performance with redesign. These approaches are used for functional testing of the parts and are not suitable for evaluation of IC performance in radiation environments.

The techniques in the second category, structured approaches, are based on the assumption that if the logic state in the latches in a circuit can be controlled and observed from the outside, then the testing problem reduces to that of testing the combinational circuit blocks that reside between these latches. The latches may not be included in the circuit design and only inputs and outputs for latches are available. In that case, latches can be introduced outside a design whenever testing is carried out. Most of the approaches in this category are based on the Level Sensitive Scan Design (LSSD) technique [14]. Other techniques that are a variation of LSSD technique are the Random Access Scan technique, the Scan Path technique, the Scan/Set Logic technique, and the Built-In Logic Block Observation technique.

For the LSSD approach, all possible inputs and outputs for all combinational circuit blocks in the circuit are connected to latches which are accessible from the outside. For testing, all input latches are loaded with test vectors for each combinational circuit block and corresponding output latches are checked for the correct response. These self-testing techniques are efficient, fast and reliable, and can be used for radiation environments to obtain information about failure. However, these self-testing techniques alone are not sufficient for radiation testing.

The above methodologies solve the problem of reducing the testing of an IC into small, manageable sections. However, due to the bias-dependency of device-parameter shifts in total-dose environments, these small, manageable circuit testing problems grow into a big problem. The worst-case testing for each small combinational circuit block must be carried out; a very difficult, if not impossible, task in itself for a VLSI circuit. The above mentioned design-for-testability approaches are aimed at functional verification of the parts, and not at radiation testing of the parts, i.e. testing in the presence of device-parameter shifts. Of course these techniques reduce the complexity of the testing task, but the level of the complexity that remains is still too high for the exhaustive level of testing required for hardness assurance in radiation environments.

Another problem with testing is the availability of results and their usefulness. Testing is usually carried out on the final product. The cost of redesigning a chip or system is related to the stage at which the necessity of redesign is discovered. This means that if the redesign is done after the final product is manufactured, the cost will be significantly higher than the cost incurred by instituting the same changes at an earlier stage. The cost incurred for redesign after a final product has been manufactured will be prohibitively high in many cases, as the redesign process will require a new design, a new mask set, and a complete run through fabrication and packaging processes for electronic parts.

In addition, the results obtained through testing are not self explanatory for radiation effects and must be meticulously analyzed to identify failure mechanisms. Results obtained from testing one electronic part are not useful for any other functionally different electronic part, even though they are manufactured from the same fabrication line.

It is clear from the above discussion that the use of self-testing methodologies does not solve the problem of testing for radiation effects. It is also intuitively clear that computer simulations of circuits do not completely (or, alone, convincingly) solve the problem of radiation-hardness

assurance either. Testing supported by the innovative methodologies for computer simulations provides a better approach to estimate the operating performance of an IC. These simulators can be used to identify the failure mechanisms and worst-case operating conditions for a given circuit operating in a radiation environment. The results thus obtained can be used along with the self-testing methodologies to efficiently assure the reliability of the parts in a radiation environment. The computer simulators currently available for circuit simulation to aid testing are discussed next.

For CMOS digital VLSI circuits, there are primarily two levels of computer simulators available for radiation environments: device-level simulators and logic-level simulators. Device-level simulators accurately simulate the circuit by calculating the accurate operating voltage for all the devices and nodes in the circuit. Logic-level simulators only simulate the ON and OFF conditions for a device in the circuit with all the nodes in the circuit being either HIGH or LOW. These two approaches and their suitability for radiation environments are discussed below.

One approach for circuit simulation is to simulate the whole circuit using conventional device-level simulators, such as SPICE [15], and to identify failure mechanisms and the worst-case operating conditions which induce these failure mechanisms. The results thus obtained can be applied to redesign the circuit if necessary. Also, by this method, failure mechanisms along with failure-exposure levels can be accurately simulated. However, the problem here is the amount of computer-hours and man-hours needed to generate the required results. Generally for a VLSI circuit, such a procedure will take a long time, and in today's market, where yesterday's technology is considered obsolete, such long delays are undesirable. The long simulation time requirements are caused by inefficient simulation algorithms for large circuits and high requirements on computer memory and computation. Also, due to bias-dependent device parameter shifts, individual device parameters for all devices must be specified.

Another way to simplify the circuit simulation of total-dose effects is to assume that all the devices experience worst-case device parameter shifts. The standard industry practice for simulating a circuit for performance in radiation environments is to obtain device-level models and assign the worst-case conditions for all devices. Under such an assumption, all p-channel devices are OFF and all n-channel devices are ON during irradiations and are assigned models accordingly. The simulations are carried out for all combinations of input conditions to obtain worst-case operating conditions after irradiation. There are several drawbacks for such an approach. First, all devices can never experience worst-case device parameter shifts at the same time due to the logical functionality of the circuit, through which the state of one device can dictate the state of another. Second, as will be shown later, such a methodology will not yield the actual worst-case combination of operating conditions during and after irradiations. Third, these simulations will still require prohibitively large number of computer-hours for complete simulations.

A better alternative is to use logic level simulators coupled with RC-delay estimation techniques to obtain the required results [4]. These types of simulators use efficient algorithms and trade accuracy of results with computation speed for enhanced performance. The term "logic-level"

implies that the circuit simulation is carried out at logic levels, namely HIGH and LOW. Information from RC-delay estimations can be used to identify the failure mechanisms and the critical test conditions. The memory and computation requirements for such an approach are extremely low as compared to device-level simulators.

The work reported herein presents a new simulator based on the above techniques for identification of failure mechanisms and reduction of test vectors for the estimation of a circuit's performance in a total-dose environment. This simulator, PARA, is based on the assumption that there are a fixed number of basic failure modes possible for a given circuit due to total-dose exposure. Circuits are analyzed using these failure mode assumptions, and fast, efficient simulation techniques are used to identify worst-case operating voltages. The results thus obtained are used to identify test vectors that will generate these worst-case operating conditions. PARA is based on the switch-level approach and uses RC delay calculations to estimate the circuit's performance and operating conditions. This methodology also includes the identification of critical sub-circuit devices solely responsible for the degradation of a circuit's performance. These sub-circuits can be simulated using more precise, slower simulators to accurately predict the circuit behavior, if desired.

2.3 SWITCH-LEVEL SIMULATION.

The switch-level simulation approach, as the name suggests, involves simulation of a digital circuit as a collection of switches. For such an approach, each device in the circuit is represented by a linear resistance in series with a switch. This approach yields an upper bound for the delays through the circuit [10].

Consider the circuit of Figure 2. Assume that the transition at the input is from HIGH to LOW. This will cause the n-channel transistor to turn OFF and the p-channel transistor to turn ON. The output node for the logic gate will rise from ground to VDD. During this process, various parasitic capacitors are charged through this p-channel transistor. Figure 2 also shows a simple model of this circuit for timing analysis. The pull-up transistor, which is non-linear, is approximated by a linear resistor. All other capacitances associated with the sources, drains, and gates connected to the output node are included in the analysis.

If all the resistances of the metal and polysilicon lines are lumped together, then all the capacitors can also be lumped together, and the circuit response may be found in closed form. The voltage at the output node is then:

$$V_{out} = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$$

where R is the pull-up resistor and C is the total capacitance at the output node. The delay, T, is directly proportional to the resistor value used. The delay, T, at which the output voltage

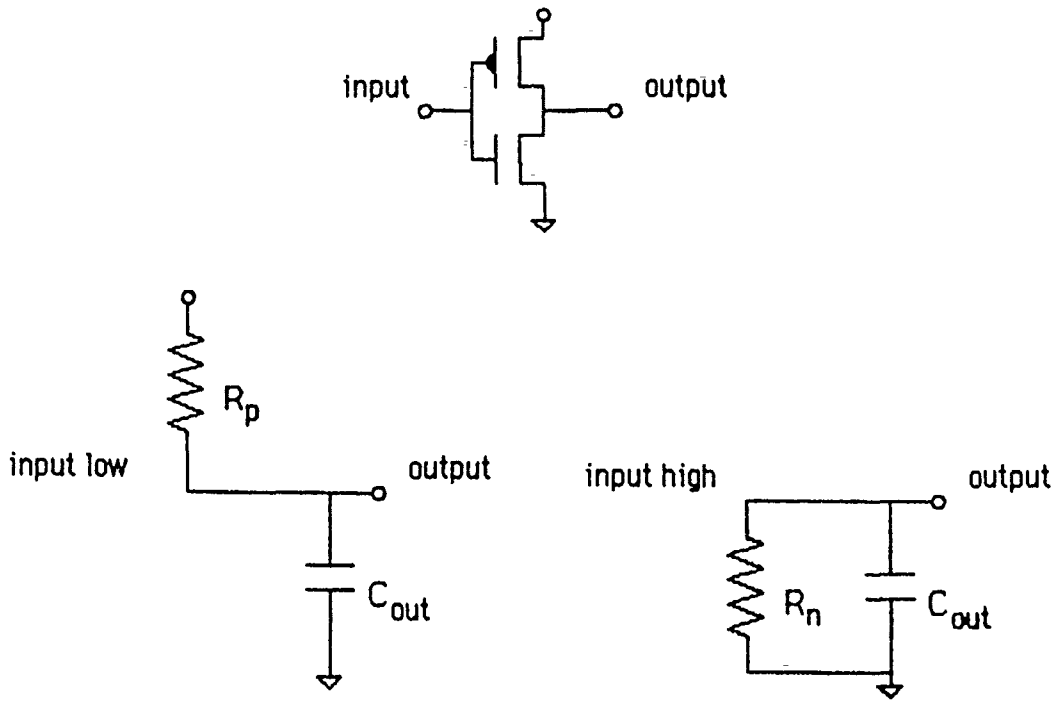


Figure 2. Models for MOS transistors for switch-level analysis.

reaches some specified critical voltage is given by:

$$T = RC \ln\left(\frac{V_{DD}}{V_{DD} - V_{CR}} \right)$$

For a CMOS circuit, the timing model is represented by a set of transistors, $T = \{t_1, t_2, \ldots t_n\}$, and a set of nodes, $N = \{n_1, n_2, \ldots n_m\}$. With each node, there is an associated capacitance, and one of the two different states corresponding to the node voltage: HIGH or LOW. One end of the node capacitor is always connected to ground, and no floating capacitors are allowed in the circuit. Each transistor has an associated ON-resistance. A transistor may be either ON or OFF depending on the input voltage at the gate of that transistor. A transistor is treated as a linear resistor with a value equal to its ON resistance if it is ON or to its OFF resistance if it is OFF. Although the capacitances and resistances for CMOS circuits and devices are operating-voltage dependent, they are treated as constants here. This approximation is considered adequate for most purposes, since only delay values are of interest and the exact waveform is not required. A MOS circuit is approximated as a sequence of RC networks, with each R and C combination representing a logic stage. Various nodal capacitances are charged and discharged through the network. This charging and discharging may change the state of a node, which in turn changes the topology of the network.

With the approximation introduced above, the problem of a timing simulation of MOS circuits reduces to that of an RC network. In this context, the term "RC network" refers only to those networks that are approximations of a CMOS circuit, i.e., resistor networks where there is a capacitor between every node and ground. In this model, it is assumed that the signal path nodes in a circuit are either HIGH or LOW, and that these are the only possibilities. Also, note that the delay models obtained using such an RC model are only as accurate as the resistance values of ON transistors. This ON resistance for an MOS device is dependent on the carrier mobility and threshold voltage.

Switch-level simulators are conceptually simple, computationally efficient, and flexible enough to handle a wide variety of CMOS VLSI circuits that are difficult or impossible to simulate using conventional simulators due to heavy computation requirements.

2.4 SIMULATION ALGORITHMS.

In this subsection, the physical characteristics of PARA are presented, and details of database and algorithms for identification of worst-case operating conditions are detailed. A flowchart for the simulation and testing methodology using PARA is shown in Figure 3.

2.4.1 Input Format.

The circuit to be tested/simulated is received by PARA in a format similar to that for SPICE. This is used to facilitate the use of PARA for large, complex VLSI circuits. For such circuits, it is extremely difficult to enter the circuit description manually in any format because of the large number of devices involved. SPICE circuit descriptions are often generated during the IC design. When they are not, software packages already available in the market can be used to convert mask layout information into a SPICE input file description. The SPICE format describes an IC in terms of transistors of varying size and types. The circuit topology is described by designating each node with a number and associating that number with terminals of all devices that are connected to it. Each transistor has four terminals, drain, gate, source, and substrate.

2.4.2 Database.

The software package, PARA, has been designed for carrying out total-dose simulations based on the failure modes discussed in the previous subsection. Various algorithms have been developed for efficient and accurate simulations. In addition, the database is designed to suit the algorithms in terms of accessibility, efficiency, speed, modularity, flexibility and portability. This insures the ease of any modifications for the inclusion of technologies other than CMOS, e.g. Bipolar, NMOS, etc. The general structure of the database is seen in Figure 4. The independence of each module from any other is seen clearly in the figure. Furthermore, the possibility of including more modules is evident from the figure. A brief description of each of the individual components is give below.

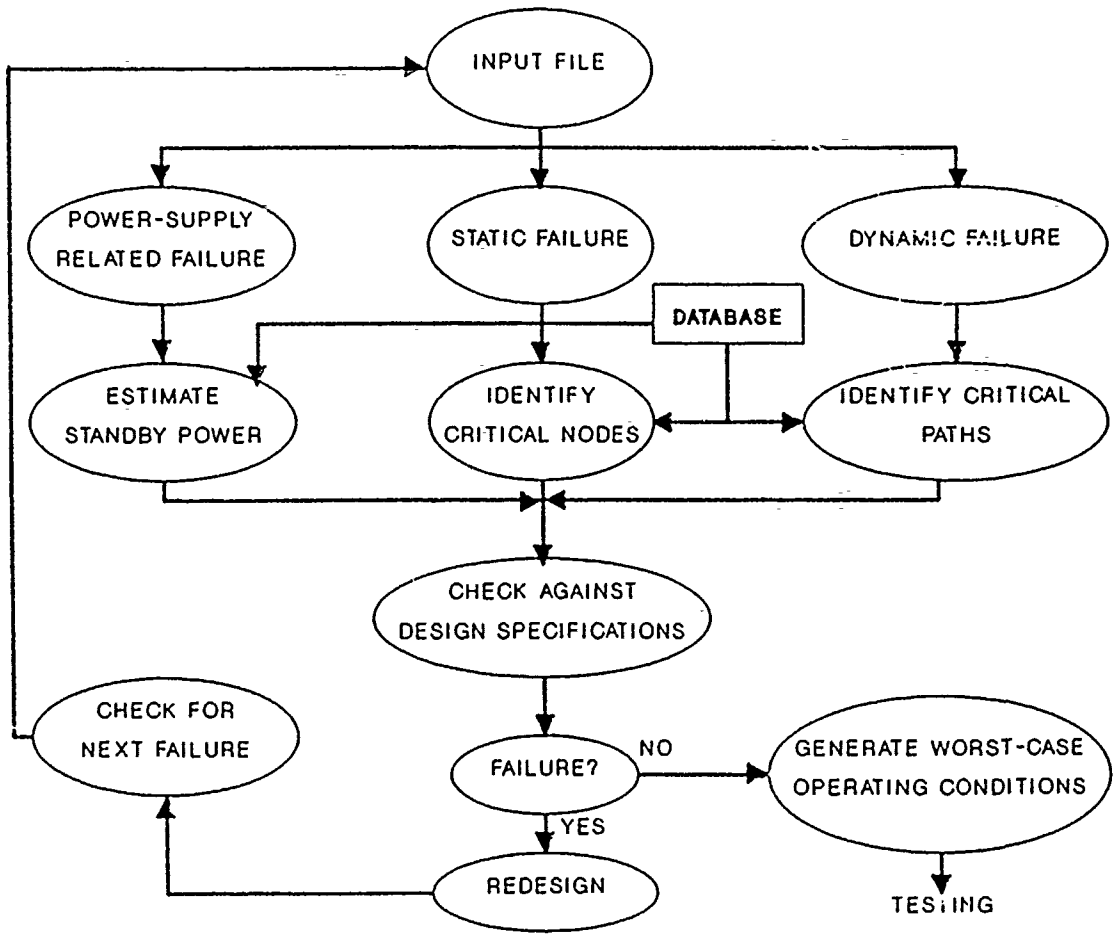


Figure 3. A flowchart for simulation process of PARA.

2.4.2.1 The Device Array. All the MOS transistor declarations in the input file are stored in this array. Each of the components of the array represents one transistor and all its attributes. The attributes constitute the four transistor terminals, size and the model parameters. All the attributes, except for the model parameters, form the private attributes. The model parameters are, in general, associated with more than one transistor, so each transistor possesses the address of the area where its model parameters are stored. More than one transistor may possess the same address for model parameters. Any transistor and its parameters can be accessed by indexing into the device array. Figure 5 depicts the structure of this memory-saving device array.

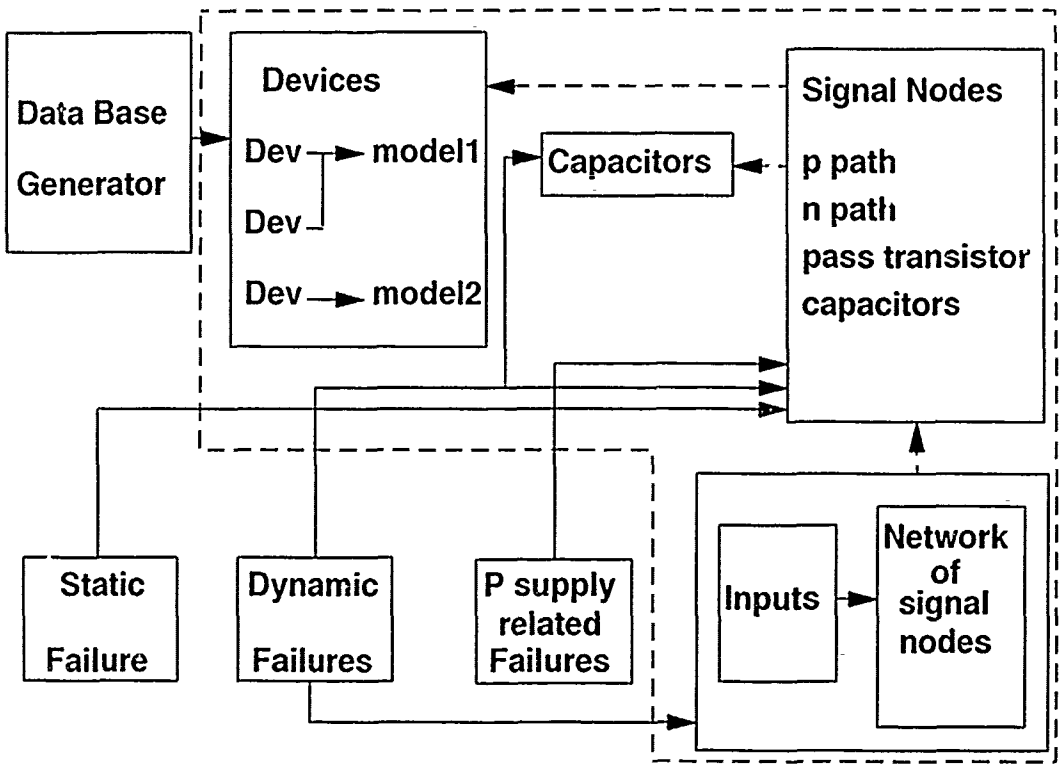


Figure 4. A database structure for PARA.

2.4.2.2 The Resistor-Capacitor Arrays. PARA stores all the resistors and capacitors in individual arrays. An individual element of these arrays would be a capacitor or a resistor with its attributes. The attributes here comprise the two terminals and the value. Figure 6 describes the array in detail.

2.4.2.3 The Model Parameters. The model parameters provided by the user are placed in a separate array. Each of the transistors has a pointer to one of the elements of the model array. Each model parameter assumes a default value until it receives a definite value from the circuit description file or .res file, discussed later.
The model array is seen in Figure 7.

2.4.2.4 Signal Node List. The list of signal nodes forms a key data structure which PARA operates on frequently. The signal nodes are extracted from the circuit description and saved in an array. A signal node essentially is an output node of a gate. This node is the only node of

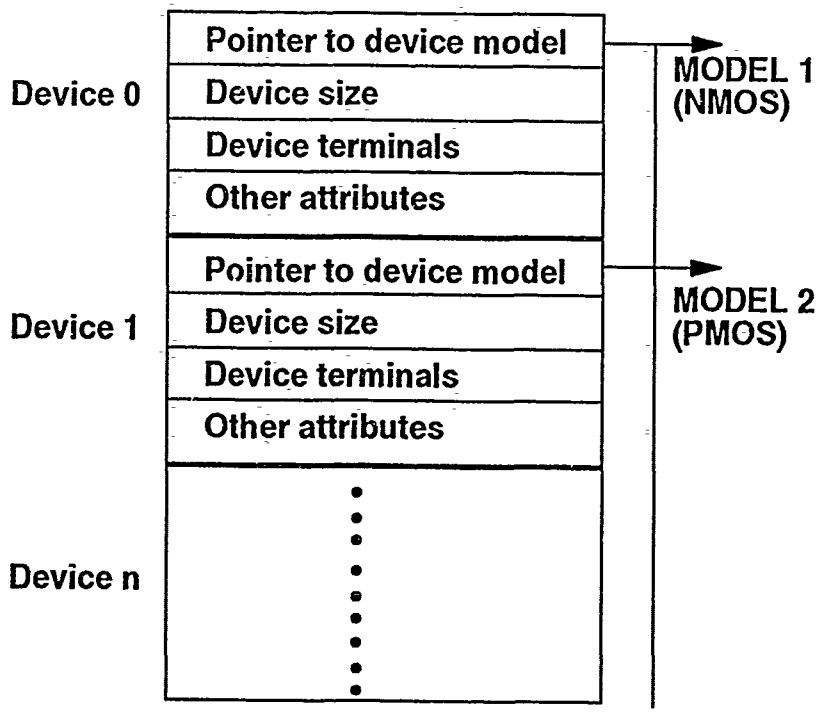


Figure 5. Device array.

interest in a gate, for digital circuits, except for the input nodes which are assumed to form the output nodes of other gates. The array element is therefore a single signal node with all the associated information. The kind of information, besides the name, appended to each node constitutes the following.

i. The path of n-channel transistors

Every CMOS gate has a series of n-channel transistors forming paths to ground. PARA stores all those n-channel transistors which form a path between the node and ground in an exact topology as they appear in the circuit. Dynamic allocation of memory is used to accommodate as many transistors as appear in the path, the limit being the memory available. The structure of the n-channel path stored is seen in Figure 3. Figure 9 depicts the components of each memory block allocated.

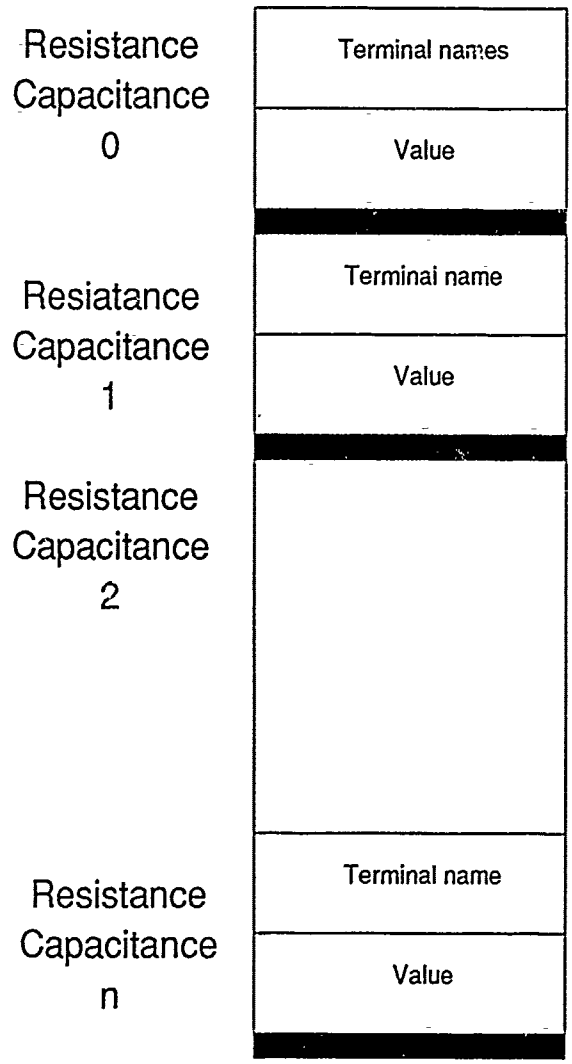


Figure 6. A model for resistor and capacitor arrays.

ii. The path of p-channel transistors
For every n-channel transistor in a gate, a p-channel transistor exists. Therefore, PARA stores a path of p-channel transistors exactly in the same fashion as the n-channel path.

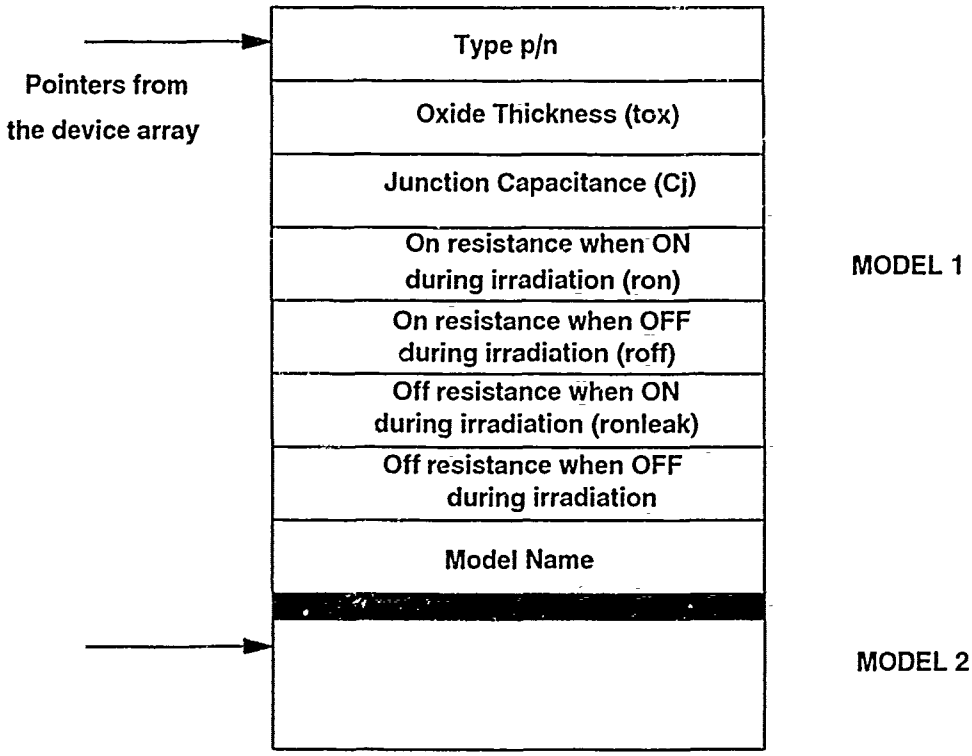


Figure 7. The model array.

iii. The path of pass transistors
A node may have a set of pass transistors (or transmission gates) which can form a path from the node to a gate of another gate. This path can be composed of n- and p-channel transistors. PARA stores this information exactly as for the other two paths mentioned above.

iv. Cumulative delays
Two arrays specifying HIGH-to-LOW and LOW-to-HIGH cumulative delays are attached to each signal node. Each of these arrays handles five maximum delays in order to test for dynamic failures. This limit can easily be increased to any number. In addition, the minimum delays are also stored for the analysis of race conditions.

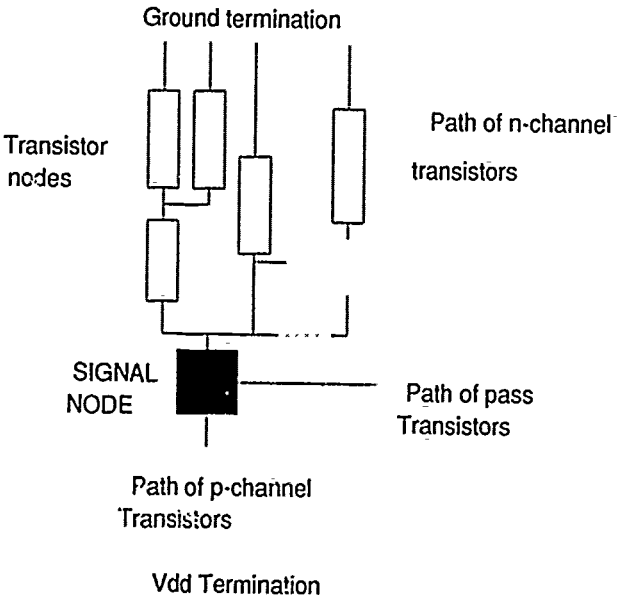


Figure 8. The structure of the n-channel path in PARA.

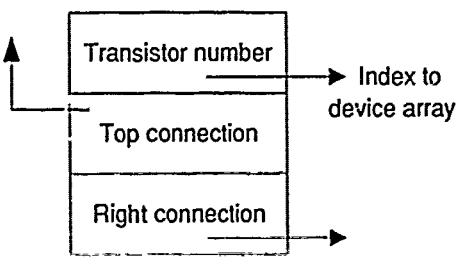


Figure 9. The structure of each memory block used.

v. Capacitance

The total capacitance at a node is the sum of all the gate capacitances, all the node (junction) capacitances and all the externally connected capacitances. These node capacitances are used for calculating delays at individual nodes and hence need to be stored.

vi. Static Degradation
The amount of static degradation at each node is also stored and the maxima are reported to the user.

There are other pieces of information associated with the nodes, but they are all for the use of internal processing and are not discussed here. A structure which depicts the nodes information is seen in Figure 10.

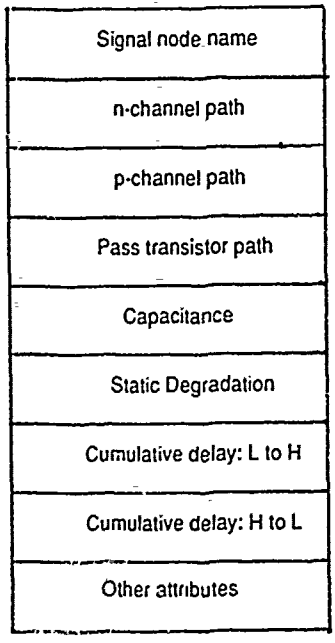


Figure 10. A model giving the nodal information.

2.4.2.5 Signal flow path. Signal_flow_path forms the topology of the circuit. All the paths representing the sequence of signal nodes forming inputs to the final outputs and inputs to latches are stored. For a three-input circuit, a signal_flow_path could look like Figure 11. The structure is a tree of nodes which point to one of the nodes in the signal node array. These nodes have three other kinds of pointers. One of them points to its children, the second points to its parent and the third points to its sibling (another child of its parent). In the figure, all the nodes connected vertically form the siblings. The nodes connected to the right of a node are its children. Since the information about the children and parent are stored, the tree is traceable in either direction. This is required for ease in the generation of signal_flow_path and for the delay calculations. The structure of an individual node is shown in Figure 12.

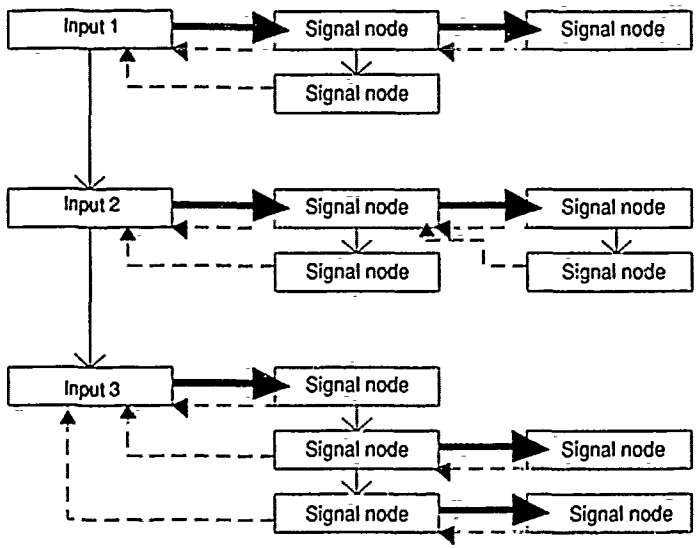


Figure 11. A signal flow path for a three input circuit.

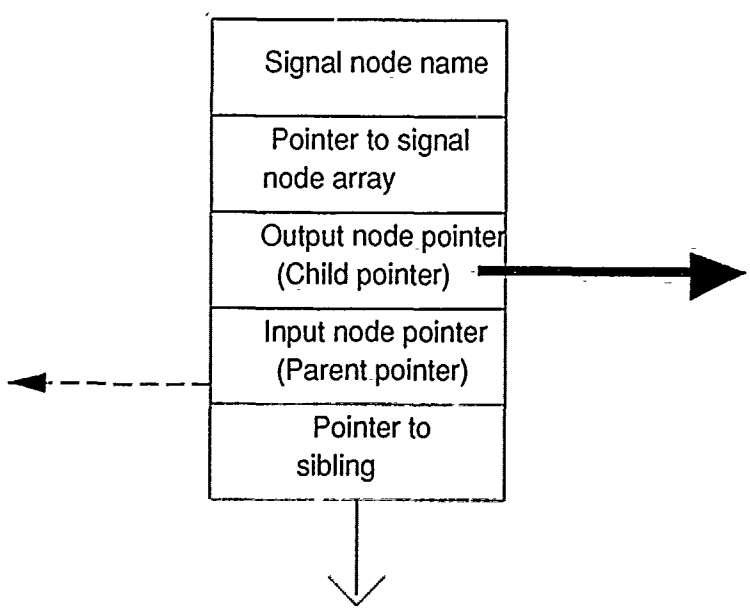


Figure 12. The structure of an individual node in a tree.

2.4.3 Algorithms.

This subsection describes all the algorithms used for the simulation of failure mechanisms.

2.4.3.1 Resistance Estimation. PARA estimates the ON resistances of devices for all cases (ON during irradiation, OFF during irradiation) by running SPICE on a chain of four inverters. Of these inverters, the last two inverters of the chain provide a good estimation of typical device resistances. The greater the number of inverters in the chain, the more accurate is the result. The accuracy, however does not increase significantly beyond four inverters in the chain. When the input goes HIGH, the output of the third inverter starts going from HIGH to LOW. At the same time the fourth inverter output goes from LOW to HIGH. The third inverter's time constant, therefore, provides the resistance of an n-channel transistor for the case when it was ON during irradiation. The fourth inverter's time constant, then, gives the resistance of a p-channel transistor for the case when it was ON during irradiation. Similarly, the falling edge at the input of the first inverter will help in determining the resistances of p- and n-channel resistances for the case when they were OFF during irradiation, using information from the third and fourth inverters respectively. The time elapsed between the input of an inverter rising/falling to 2.5 volts and the output of the inverter falling/rising to 2.5 volts was found to be the most suitable time constant for resistance calculation through trial and error method. In order to suppress the effect of internal node and gate capacitances, large capacitances (10 pF) are added at each node during this calculation. Therefore, these capacitances that determined the time constants rather than the internal device capacitances. The resulting time constants are divided by these capacitances to compute in the average resistance of the transistor.

2.4.3.2 Static Degradation Estimation. This involves the following steps:

For every signal node:

i. Determine the minimum "pull up" path. This can be done by looking at the path of p-channel transistors and extracting the one that has the maximum resistance. For most cases, the path is formed by the maximum number of p-channel transistors connected in series between the signal node and VDD. In Figure 13, the path formed by Q2 and Q3 is the minimum pull up path. The higher of the two possible resistances (ON during irradiation and OFF during irradiation) is taken for all the transistors in the path.

ii. Add all the resistances in the minimum pull up path resistance (Rp).

iii. Determine the resistance (leakage) for the n-channel path corresponding to the pull up path found. Q4 and Q5 form the maximum leakage path for the above pull up p-channel path.

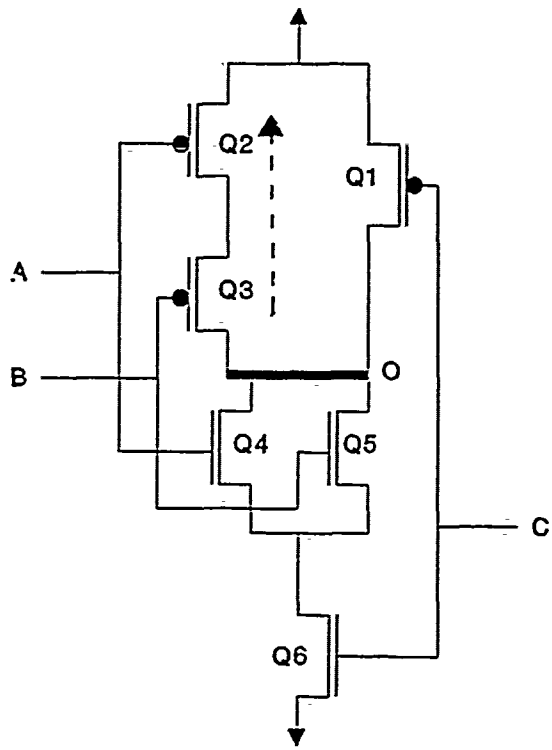


Figure 13. An example showing minimum pull up path.

iv. Take the parallel combination resistance (Rl) of all such n-channel transistors. (They are always in parallel.)

v. The degradation at the node, which is the maximum deviation from the supply voltage level, is given simply by the following formula.

$$\text{Degradation} = VDD[1 - Rl/(Rl + Rp)]$$

The nodes having the maximum values of degradations are reported to the user.

2.4.3.3 Dynamic Degradation Estimation. The steps involved are the following:

For every signal path:

i. Take the first node in the signal path.

ii. Assume the input was HIGH during irradiation and goes from LOW to HIGH after irradiation. This could make only one change in the corresponding output node, i.e. change from HIGH to LOW.

iii. If the node has already been visited in this path (loop), break this path and go to the next one.

iv. If the node is going from HIGH to LOW calculate the maximum n-channel resistance to ground by going through the path of n-channel transistors associated with the node. The product of the node capacitance and the equivalent n-path resistance calculated gives the delay for this node. In case the node is going from LOW to HIGH, the maximum pull up resistance through the path of p-channel transistors is used to calculate the delay. In addition, the maximum resistances of all the pass transistors connected to the node are added. This gives a complete delay for the signal to reach the input node of the following gate(s).

v. Add this delay to the previous delay at the previous node to obtain the cumulative delay at this node. If the cumulative delay at this node calculated through some other path is more than the new cumulative delay, ignore this new delay and go to the next path. If the previous node is an input node, then the previous delay is 0.

vi. Go to the child of this node (output node for this node, as described in database subsection above) and repeat the above steps.

vii. Go to the sibling of this node and repeat the above steps.

viii. Go to the next path. If all the paths have been traversed, stop. Repeat the above steps for three other cases: when the input was HIGH during irradiation and goes from HIGH to LOW after irradiation, the input was LOW during irradiation and goes from LOW to HIGH after irradiation, and the input was LOW during irradiation and goes from HIGH to LOW after irradiation.

The paths associated with the nodes of highest delays are the critical paths for dynamic failures.

2.4.3.4 Power Supply Related Failure. The following steps are followed:

For all nodes in the circuit:

i. Assume the node to be HIGH, since the leakage at LOW nodes is negligible.

ii. Determine the minimum OFF resistance (R) of the node to ground by traversing the path of n-channel transistors connected to the node. VDD/R gives the leakage current from the node. Add all the leakage currents and divide by 2 to get the average leakage current. This assumes that half of the nodes are HIGH at any particular moment.

The above database and the algorithms form the kernel of PARA. Other procedures present are related to the input and output handling for maximum user friendliness. The appendix describes some of the files that contain these procedures.

2.5 SIMULATION RESULTS.

In this subsection, results of simulations performed on several CMOS digital circuits using PARA and SPICE are presented. The test circuits are chosen to represent a wide range of functions and desigr methodologies varying from an inverter chain to an 8-bit full adder circuit. The number of transistors varies from 24 to 1300.

For all the following simulations, it was assumed that dynamic failure will occur if the delay for the worst-case path increases by more than 20%. The static failure is assumed to have occurred if the p-path devices fail to raise the output node higher than 3.0 volts with supply at 5.0 volts. Due to small number of devices involved, the operating current failure is not possible for these circuits. Hence, that type of failure simulations did not report failures. For actual analysis, all possible combinations were considered to verify that the worst-case conditions reported by PARA are indeed worst-cases.

2.5.1 Inverter Chain.

The circuit tested contained 12 stages of inverters with fanout of 1 at each stage. The capacitance values at each node were kept the same except for the input and the output node. PARA predicted that the inverter chain will not fail due to the power supply-related failure or static failure. This is obvious in this case as all the stages were designed using properly ratioed logic to remove static failures. The power consumed by the 12-stage inverter chain is never high enough to cause any problem with power supply overload or heat dissipation. PARA correctly predicted the failure mode to be a dynamic failure mode, i.e. the inverter chain will fail because the input signal will experience increased delay after irradiation and this delay may be high enough after certain exposure threshold to cause a malfunction. A hypothetical failure was assumed to have occurred when the increase in the delay through the inverter chain was greater than 20% of the original value for simulation purposes. Simulation results for the dynamic failure are presented in Table 1 along with the results from SPICE for comparison purposes. PARA took less than a second to obtain these results while SPICE took 95 seconds of CPU time to simulate only the worst-case path with one set of bias conditions.

For a simple circuit like an inverter chain with an even number of stages, two combinations of operating conditions provide complete simulation coverage, due to the even number of stages: input HIGH during irradiation and switching from HIGH-to-LOW for simulations after irradiations or input HIGH during irradiations and switching from LOW-to-HIGH for simulations after irradiations. Table 1 shows results obtained for both the cases using SPICE and PARA. The input LOW during irradiations and LOW-to-HIGH and HIGH-to-LOW transitions after irradiations are equivalent to the above conditions.

As expected, the results clearly show that the inverter chain will have highest delay associated with it when the input signal faces worst-case conditions at each stage. This means, if the input

Table 1. Results of simulation.

input		delay in nsec		% increase in delay	
during	after	SPICE	PARA	SPICE	PARA
*low	h → l	5.28	5.32	20	21
low	l → h	4.90	4.99	12	13.5
high	h → l	4.90	4.99	12	13.5
high	l → h	5.28	5.32	20	21
all max	h → l	4.95	4.84	12.5	10

was held HIGH during irradiations, the worst-case delay for the chain is obtained for the HIGH-to-LOW transition at the input. For the complimentary transition of LOW-to-HIGH, the signal path faces less than worst-case conditions, and hence, the increase in the path delay is smaller than the path delay for the worst-case conditions.

The current industry method of obtaining worst-case conditions is to assign worst-case delay to all the devices, i.e. assume all p-channel devices to be OFF and all n-channel devices to be ON during irradiation, accordingly assigning device parameter shifts, then carry out simulations for all possible transitions at inputs. For such a case, the increase in the path delay is much smaller than the worst-case delay as shown in Table 1.

2.5.2 4-Bit Carry Look-Ahead Circuit.

This test circuit is a high speed, look-ahead carry generator capable of anticipating a carry across four bit binary adders. PARA took about 15 seconds to simulate the circuit while SPICE needed 129 seconds just to simulate only the worst-case path for one set of bias conditions. A designer would need to run the same simulations 2^9 times, as the number of inputs is 9, to obtain results reported by PARA.

PARA correctly predicted that the failure mode will be dynamic. Static failure does not occur until n-channel devices were operating in depletion mode. This is true for most designs as only a small number of n-channel devices are associated with each signal path node. The increase in leakage under irradiation will not be extremely high. For dynamic failure, the increase in the worst-case path delay was observed to be more than 20%. The simulation results using PARA and SPICE before irradiation are shown in Table 3 for comparison purposes. The post-irradiation

simulations are shown in Table 4. Only two set of operating conditions are shown: all inputs HIGH during irradiation and switch from HIGH-to-LOW after irradiation, and all inputs LOW during irradiation and switch from LOW-to-HIGH after irradiation. All possible paths for these operating conditions are shown. From all such possible simulations, the worst-case path is chosen and is shown in Table 2. The results for the second most worst-case path, a random path, and worst-case path with equal device parameter shifts are also shown in Table 2. These results clearly show that the increase in delay for the worst-case path using proper bias conditions during and after irradiations is significantly higher than for any other bias conditions. SPICE results are in clear agreement with results obtained using PARA. Worst-case device parameter shifts for all devices proved not to be the worst-case for the given circuit.

To prove the validity of PARA algorithms, we designed an experiment to carry out the actual radiation exposure on various circuits. The test circuit chosen was 4-bit look-ahead carry generator due to its size and circuit complexity. We designed four different circuits implementing the same function using only 2-input NAND gates, 2-input NOR gates, only 2-input gates, and multi-input gates. These designs required 214, 233, 222, 180 gates respectively. The layouts for these designs were generated at Vanderbilt and the IC was fabricated at MOSIS foundry service, using their non-hardened, n-well, 2.0 μm, CMOS process. The IC was irradiated using a Co60 source at Vanderbilt at 40 kRads(Si) per hour.

Simultaneously, PARA was run on these circuits to identify the worst-case conditions and circuit-parameter degradations. During the first exposure experiment, the circuits were biased at worst-case conditions (obtained from PARA) for all four designs. For the second experiment, bias conditions other than worst-case were used. The resultant degradations in circuit parameters are given below in Figure 14 and 15. As can be seen from the experimental results, PARA correctly identified the worst-case bias conditions for all circuits.

Table 2. Simulation results for carry look ahead example.

input		% change in delay	
during	after	SPICE	RC
*high	h – l	22	20.7
high	l – h	4.8	4.1
low	h – l	5.2	4.1
low	l – h	17.7	17.7
all max	h – l	6.5	7.9
all max	l – h	7.2	8.1

Table 3. Simulation results.

path number	input transition	simulation results	
		SPICE	PARA
1	l → h	3.2	3.24
2	l → h	2.5	2.54
3	l → h	2.3	2.30
4	l → h	2.0	2.00
5	l → h	2.0	2.00
6	l → h	2.0	1.98
7	l → h	2.0	1.98
8	l → h	2.0	1.98
9	l → h	2.0	1.95
10	l → h	2.0	1.95
11	l → h	2.0	1.94
12	l → h	2.0	1.92
13	l → h	1.8	1.88
14	l → h	1.8	1.86
15	l → h	1.7	1.74
16	l → h	1.7	1.73
17	l → h	1.7	1.72
18	l → h	1.7	1.69
19	l → h	1.7	1.68
20	l → h	1.7	1.68
21	l → h	1.7	1.66
22	l → h	1.7	1.66
23	l → h	1.5	1.49
24	l → h	1.5	1.48
25	l → h	1.5	1.47
26	l → h	1.5	1.46
27	l → h	1.5	1.45
28	l → h	1.4	1.43
29	l → h	1.4	1.42
30	l → h	1.3	1.26
31	l → h	1.3	1.25
32	l → h	1.3	1.25
33	l → h	1.2	1.23
34	l → h	1.2	1.21
35	l → h	1.2	1.20
36	l → h	1.2	1.18
37	l → h	1.2	1.17
38	l → h	1.1	1.13
39	l → h	0.7	0.56
40	l → h	0.7	0.56
41	l → h	0.7	0.56
42	l → h	0.7	0.56

Table 4. Simulation results for carry look ahead example.

path number	input transition		simulation results	
	during	after	SPICE	PARA
1	low	l → h	3.7	3.74
2	low	l → h	3.1	3.12
3	low	l → h	2.8	2.83
4	low	l → h	2.7	2.65
5	low	l → h	2.7	2.64
6	low	l → h	2.7	2.62
7	low	l → h	2.7	2.62
8	low	l → h	2.7	2.62
9	low	l → h	2.6	2.59
10	low	l → h	2.6	2.58
11	low	l → h	2.6	2.57
12	low	l → h	2.6	2.54
13	low	l → h	2.6	2.49
14	low	l → h	2.6	2.46
15	low	l → h	2.2	2.28
16	low	l → h	2.2	2.28
17	low	l → h	2.2	2.25
18	low	l → h	2.2	2.23
19	low	l → h	2.2	2.22
20	low	l → h	2.2	2.21
21	low	l → h	2.2	2.19
22	low	l → h	2.2	2.18
23	low	l → h	2.0	1.93
24	low	l → h	2.0	1.92
25	low	l → h	2.0	1.91
26	low	l → h	2.0	1.89
27	low	l → h	2.0	1.89
28	low	l → h	2.0	1.86
29	low	l → h	2.0	1.85
30	low	l → h	1.6	1.62
31	low	l → h	1.6	1.60
32	low	l → h	1.6	1.60
33	low	l → h	1.6	1.58
34	low	l → h	1.6	1.55
35	low	l → h	1.6	1.54
36	low	l → h	1.5	1.51
37	low	l → h	1.5	1.50
38	low	l → h	1.5	1.45
39	low	l → h	0.7	0.73
40	low	l → h	0.7	0.73
41	low	l → h	0.7	0.73
42	low	l → h	0.7	0.73

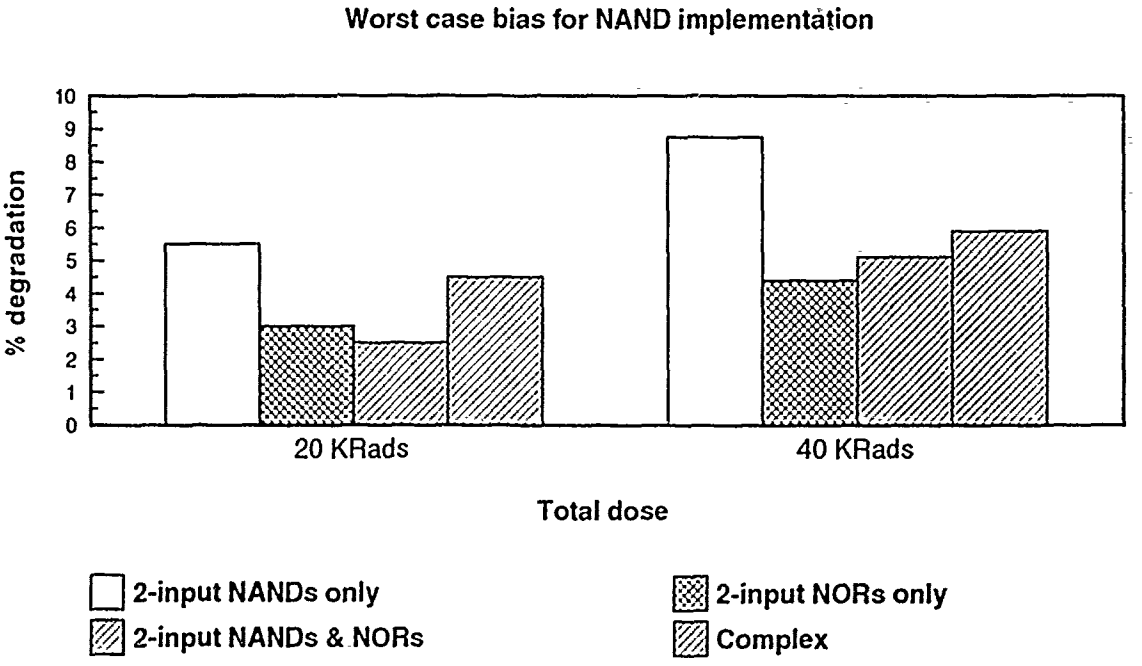


Figure 14. The effects of different topology but same bias conditions on radiation degradation.

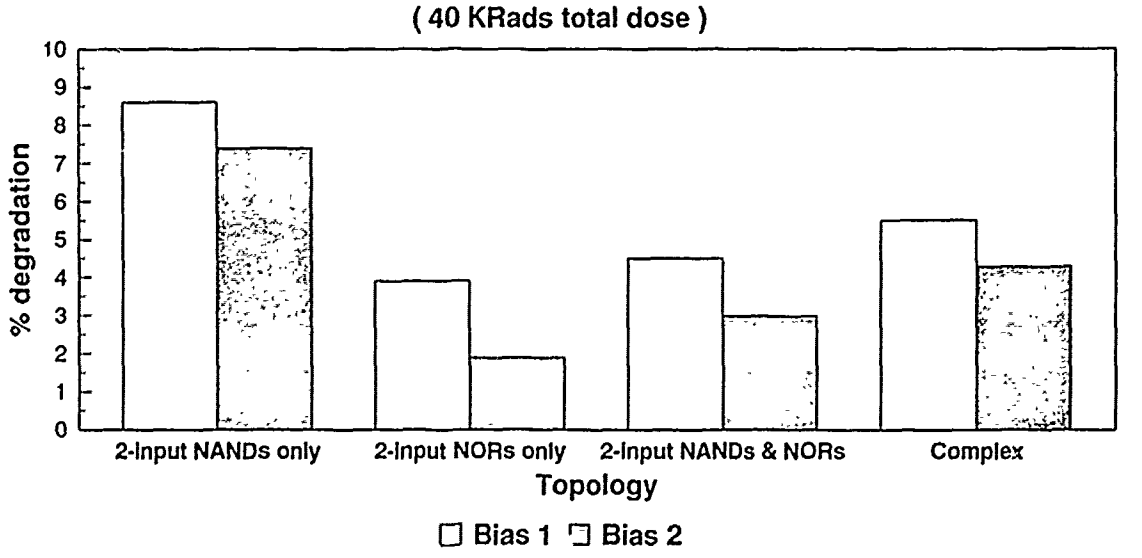


Figure 15. The effects of different bias conditions on same design for radiation degradations.

2.5.3 Static Random Access Memory Column.

This circuit contains about 500 CMOS transistors. The function of the circuit is to store and extract the memory bits as required. The column includes memory cells along with peripheral and sensing circuits. Conditions for failure detections are same as mentioned previously. PARA required 45 seconds of CPU time while SPICE required 3000 seconds of CPU time for one simulation run.

The failure for this circuit was determined to be due to the static failure mode. PARA predicted the failure will occur for the operating conditions as shown in Figure 16. During irradiation, all memory bits maintained same state. For post-irradiation tests, one of the memory cells was flipped. The resultant memory pattern causes static failure, due to increased leakage on the bit line. When the sensing circuit tries to read the memory cell whose state was complimented after irradiation, the leakage current due to all other memory cells and peripheral circuits proves too much for the small memory cell devices to pull the bitline high enough for a proper read operation. This type of failure has been experimentally observed and simulated using SPICE.

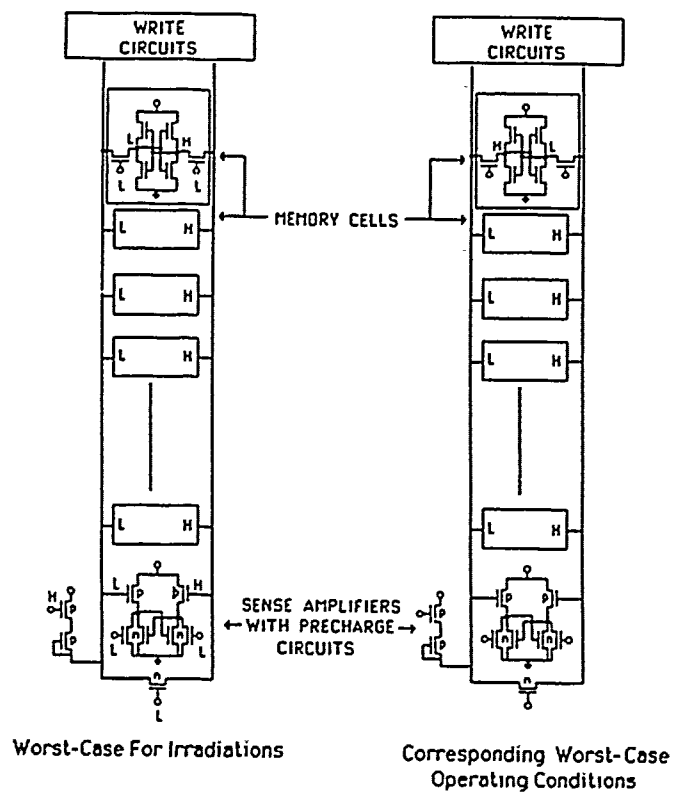


Figure 16. Worst-case bias conditions for memory cell example.

For any other combination of memory cell inputs, such as the industry-standard checkerboard pattern where alternate memory cells contain complimentary states, the failure mechanism proves to be fabrication-process dependent. For some fabrication processes, failure was attributed to shifts in sensing circuit devices, while other circuits failed due to "imprinting" of the logic states.

The experiments clearly showed that for checkerboard patterns, the memory column fails at higher radiation exposure than for true worst-case bias conditions.

2.5.4 8-Bit Full Adder.

This is part of an arithmetic logic unit of a microprocessor. The circuit was made up of about 1300 p-channel and 1300 n-channel devices. SPICE simulations were performed only on parts of the circuit due to heavy requirements on CPU time.

The failure mode again was discovered to be dynamic failure mode. The worst-case operating conditions along with some of the other conditions for worst-case delay path is shown in Table 5. Some of the other paths are also shown for comparison purposes. All the above results obtained from SPICE and PARA show that accurate failure simulations are possible using mixed-mode simulators and SPICE. The mixed-mode simulation method is much faster and more efficient than the conventional simulation method as evidenced by results of simulations presented above.

Table 5. Simulation results for 8-bit full adder circuit.

Dynamic Failure Mode			
input		% change in delay	
during	after	SPICE	RC
*low	l → h	34.7	29.7
low	h → l	8.8	10.1
high	h → l	25.3	22.1
high	l → h	10.7	8.7
all max	all max	14.5	16.3

2.6 CONCLUSIONS.

PARA can be used extensively in analyzing the performance of CMOS digital ICs as a function of the device parameters. Fast and accurate timing analysis can easily be used before deploying the circuits in the field. The maximum benefit comes to the ICs which need to be used in radiation environments. The performance of ICs for various radiation levels can be assessed automatically and with considerable ease. Other effects which directly affect the device parameters, such as temperature, can also be easily simulated.

PARA is designed to have maximum modularity in order to provide for future extensions. Other types of radiation effects, such as single-event upsets and prompt dose effects, can be incorporated into the PARA structure. Useful features, including infant failure analyses and automatic test vector generation can be included without much difficulty.

SECTION 3

SINGLE-EVENT UPSET MODELLING OF SILICON-ON-INSULATOR TECHNOLOGIES

3.1 INTRODUCTION.

During this contract period, the Vanderbilt Space Electronics Research Group has been involved in the modelling and simulation of single-event radiation effects on silicon-on-insulator (SOI) technologies. It was desired to determine the dominant fundamental mechanisms leading to static random-access memory (SRAM) upsets in these technologies. The study included the interaction of the charge track with the thin silicon material, the transient effect on parasitic devices, and the incorporation of these effects into a lumped-element macro circuit model for upset simulations in TRIGSPICE [36].

As a result of this work, we feel that several contributions to the understanding of single-event phenomenon in SOI circuits have been made. In terse outline form, these contributions are:

1) It was found that the parasitic bipolar devices inherent in any SOI MOS technology can be triggered by the local charge deposition of a cosmic ion. The charge enhancement created by the gain of this bipolar device can significantly effect the upset characteristics of a SRAM cell.

2) Electrical connection of the body region to the source region (body ties), used to keep the body region from floating during normal device operation, can often be yielded ineffective by the single-event pulse. Due to a *local* charge injection by the cosmic ion, the intrinsic body resistance can help create a local transient bias which can lead to minority carrier injection into the body at that localized point and a bipolar action.

3) Empirical modelling of the nonlinear H_{fe} versus V_{BE} curves for the parasitic bipolar is critical for accurate SEU simulations.

4) The macro model developed is very computationally efficient, yet yields excellent upset simulation capabilities.

5) We have used the model to study the effects of body resistance, device width, number and placement of body ties, and material parameters on single-event upset rates.

During this contract period, two students have completed degrees directly related to this work. Michael Alles completed his Masters Degree with a thesis entitled: "A Lumped-Element Model for Simulation of Single-Event Radiation Effects on Small Geometry Silicon-on-Insulator Transistors". Mike worked on the model development and SEU critical charge simulations. Laura Edwards completed her Masters Degree with a thesis entitled: "Prediction of Single Event Upset Rate in CMOS SOI." Laura worked in the area of applying existing upset rate codes to SOI

technologies. A great majority of the following descriptive report is excerpted from the thesis of Michael Alles, which presently is the most complete and extensive documentation of our SOI modelling work.

3.2 SOI SINGLE-EVENT DEVICE MODEL DEVELOPMENT.

This subsection will present the development of a lumped-parameter model for simulation of single-event radiation effects on SOI transistors in which the source/drain diffusion extends completely to the underlying oxide (fully bottomed junctions). The devices which are studied and modeled are not fully depleted structures [37] . This means that when the MOS device is turned "on", the entire body region is not depleted, and some quasi-neutral region exists. The devices do have the body electrically contacted to the source, although the model is applicable to devices which have no body contacts (floating body). The model is developed based on the physical structure and characterization data taken from SOI test transistors and is implemented in the SPICE circuit simulator. The first subsection will discuss the type of data error with which this work is concerned. The following subsection will establish the general criteria for the model development and overview the literature reporting on work which has been done on SOI device modeling and simulation. The device structure and physical characteristics along with the ion-device interaction process is then described. Of particular interest are the differences between ion effects in SOI and bulk type CMOS devices. In the final subsection, the SOI device model elements are identified.

3.2.1 General Model Considerations.

In order for simulation to be a practical design tool with today's large integrated circuits, the simulator and device models used must be simple enough to allow adequate computational efficiency and convergence of multiple device simulations, while maintaining sufficient accuracy to adequately predict device and circuit performance in complex radiation effects simulations. Although 2 and 3 dimensional simulators (such as PISCES) may give accurate and insightful results for a single device or small number of devices, they become impractical for larger circuits and SEU simulations due to memory requirements, CPU time, and complexity. For this reason, a one dimensional simulator such as SPICE is preferable. In addition, a lumped parameter modeling approach is chosen for efficiency (simulation time and memory requirements) and simplicity of model implementation.

It has been established that SOI IGFETs (isolated gate field effect transistors)demonstrate characteristics different from conventional IGFETs fabricated on silicon substrates [38-40] due to structural differences. Because of this, standard bulk MOSFET models do not adequately represent the SOI MOSFET device performance. Even when bulk model parameters are fit to experimental SOI-FET transistor curves, simulations have shown substantial error in device and circuit responses [41]. SOI-FET transistors require a more elaborate description in which device characteristics are dependent on the mode in which the device is operating as well as on the individual device structure.

Much work has been done on SOI device level characterization, both experimentally and analytically, and an increasing amount of experimental effort is going into circuit level radiation effects analysis in order to develop designs which are less susceptible to radiation [42-43]. In particular, the majority of the radiation effects characterization has dealt with other types of radiation effects (dose rate and total dose) since the structure of the SOI devices inherently provide an increased degree of immunity to single-event effects over bulk CMOS devices as discussed in the next subsection.

Models currently available, which address the unique properties of SOI devices, have been studied for the purpose of modeling and simulation of single-event radiation effects on SOI transistors. Although the models accurately model SOI transistor performances under normal operating conditions, they generally do not incorporate the modes of operations which may become active when the devices are subject to single-event effects [44]. These modes of operation are not active during normal device characterization, and usually are more difficult to model. In particular, the lack of accounting for parasitic bipolar properties in SOI models [45] is a major concern for SE simulations. While it is true that the parasitic bipolar is not significant for modeling normal device operation, it becomes a major factor in modeling single-event effects as will be discussed in the following subsections. In addition, even for modeling normal operating conditions, the models appear complex both numerically [46-48] and computationally [49-53] or are limited in device structures or range of operating conditions [54-57]. More recent characterization and modeling efforts have concentrated on the optimization of device designs and the effects of scaling the SOI devices to smaller device sizes and thinner active layers [58-61], but again the concentration is on normal device operation or post irradiation operation (for example, increases in leakage currents and shifts in threshold voltages [43,60]).

3.2.2 Device Structure and Charge Collection.

CMOS-SOI devices are distinguished from bulk MOS devices by a decreased charge collection volume reducing the direct perturbation of the device during the penetration of an ion (single event). The charge collection volume in bulk MOS devices extends into the substrate via "funneling" [62]. Figure 17 shows a 3 dimensional view of an n-channel SOI device with fully bottomed junctions, meaning that the source and drain diffusion extend to the insulating oxide layer. In this structure, the charge collection volume (depth) is truncated by the oxide. While this decreased charge collection volume lowers the charge collected from direct ionization, another mechanism of charge enhancement exists.

In the isolated body structures (fully bottomed junctions), carriers which are generated by ionization in the channel of an "off" device may 1) recombine, 2)be collected within depletion regions, or 3) act as current injected into the base of the bipolar structure, that is diffuse to the junctions (aided by the weak field outside the depletion regions) and initiate bipolar action. All of these processes also occur is bulk CMOS, but the dominant effect driving upset is the

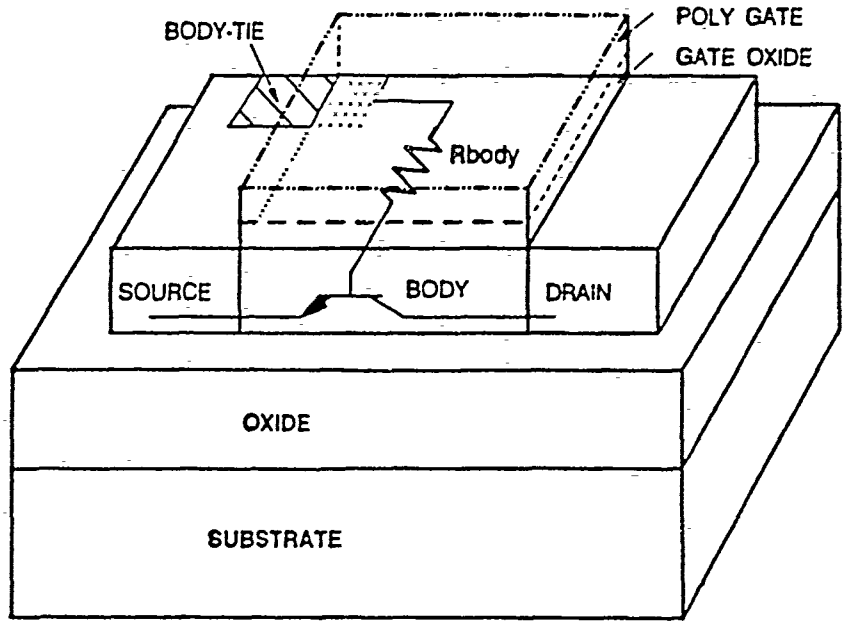


Figure 17. N-channel SOI device 3-dimensional representation.

depletion collection via charge funneling; the other effects are negligible. We have found that in SOI devices, all of these three effects are important and must be accurately modelled. Outside a diffusion length from the drain depletion region, current generated due to ionization is removed as substrate current or recombines. In isolated body SOI structures, direct ionization current is not the major contribution to upset because the collection volume is greatly reduced by the underlying insulator. It is assumed that the collection region does not extend into the substrate and funneling is not significant. This is a reasonable assumption since the carrier mobility of the insulator is so low and since the depletion region would not extend into the insulating oxide to collect any ionized charge which may be generated. It is the parasitic lateral bipolar structure which is the dominant mechanism of charge enhancement. Ionization generated minority carriers within a diffusion length of the collector depletion region induce photo current at the collector junction. This photo current removes minority carriers from the base (body) thus causing minority carrier injection at the emitter junction i.e bipolar action. Thus the isolated body device acts as a bipolar transistor with a floating body and the ion induced photo-current provides the base current. Measurements associated with the bipolar structure taken on test devices confirm that bipolar action can occur in these devices if the body-source (base-emitter) junction becomes forward biased.

3.2.3 SOI Single-Event Model Elements.

In Figure 17 the drain-body-source (n-p-n) structure forms the parasitic lateral bipolar structure which may become active if the body-source (or body-drain) junction becomes forward biased [63-64]. In practice, it is common that the body region is contacted to the source via a low resistance "body-tie" in order to keep this junction from becoming forward biased. Although this effectively inhibits bipolar action under normal operating conditions, an ion penetrating the transistor body (bipolar base) may induce sufficient ionization charge to cause some portion of the body-source junction to become temporarily forward biased. During a single event, the potential at points within the body can be higher than that at the body-source contact because ion-induced current must be drawn through the resistance of the lightly doped body material between the contact and any region within the body. This resistance, shown in Figure 17 as Rbody, along with the body-source and body-drain junction capacitances form an RC circuit such that the time necessary for the ion-induced photocurrent to be removed by the body-tie is greater than that necessary to initiate bipolar action (corresponding to a diffusion length from the body-drain junction).

From this structure, the device model elements can be identified. The overall structure can be modeled as an MOS (accounting for the majority carrier channel current and junction, gate and overlap capacitances) and a BJT (accounting for the minority carrier bipolar currents, non-ideal junction diode characteristics, and diffusion capacitances) having common drain-collector, source-emitter, and body-base nodes respectively. Drain (collector) and source (emitter) resistances should appear extrinsic to the MOS and BJT to properly model these common nodes. A resistance (Rbody) is inserted between the body and source nodes in modeling devices which have body-to-source ties. A drain to source shunt resistance may be added to model non-ideal leakage of poor quality devices. The p-channel SOI model thus consists of a p-channel MOS and a pnp BJT while the n-channel SOI model consists of an n-channel MOS and a npn BJT, along with the noted resistances. Details of the model implementation and determination of model parameters are discussed in the following subsection.

3.3 IMPLEMENTATION AND PARAMETERIZATION.

In this subsection, the implementation of the device model and the determination of model parameter values are discussed. The model is implemented in the TRIGSPICE [36] circuit simulator. The implementation is straightforward but does require some modification of the TRIGSPICE code. The model is divided into three sections which must be parameterized: the MOSFET, the BJT, and the body resistance. An additional resistance may be necessary in some cases to model leakage. The measurements and procedure used to determine parameters for each section are described. In addition, the current pulse used to model the photocurrent induced by the ion penetration is described.

3.3.1 Device Model Implementation.

Figure 18 shows the model for an n-channel device developed for simulation c. . .gle-event vulnerability of SOI transistors. The model includes the body resistance (Rbody) and emphasizes the effect of the parasitic bipolar structure. The resistance, Rleak, may be used to model non-ideal leakage of the OFF device. (The p-channel model is obtained by replacing the NMOS with a PMOS and the npn by a pnp.)

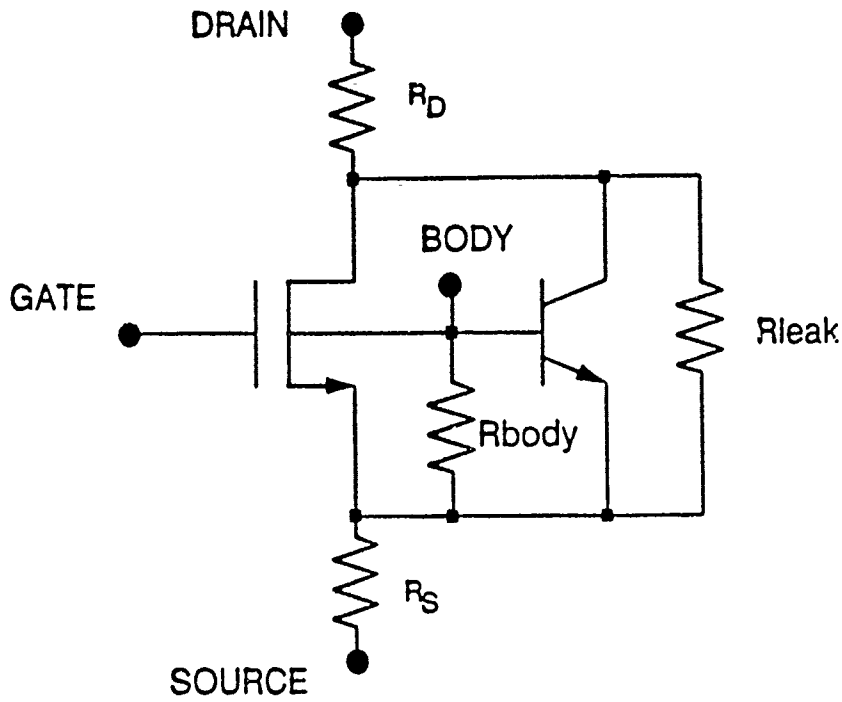


Figure 18. N-channel SOI/SEU device model for SPICE.

In imp. .enting this SOI model, the device is divided into two major components: the channel current and capacitances associated with the MOS, and the bipolar currents and non-ideal junction diode characteristics associated with the parasitic bipolar structure. The two models, as shown in Figure 18, are connected in parallel with the body node of the MOSFET model connected to the base node of the bipolar model. This configuration creates a redundancy in that the junction diodes appear in both models. It is therefore necessary to remove the ideal junction diodes intrinsic to the MOSFET SPICE model. This required some modification of the TRIGSPICE code. Prior to the modification, the diodes could not be deactivated. Setting one of the saturation current parameters (IS or JS) to zero caused TRIGSPICE to use default values. With the modification, a zero value for IS or JS will cause the diodes to be deactivated. The bipolar model has more sophisticated diodes which can represent non-ideal diode characteristics. This model is used to replace the junction diodes of the MOS model thus allowing the parasitic bipolar gain

characteristics to be fit to those measured from devices. The drain and source resistances in the MOS model and the collector and emitter resistances in the bipolar model are set to zero so that the bipolar model appears properly in parallel with the MOS model. The SOI lumped-parameter model drain and source resistances are included extrinsically as shown in Figure 18. A resistance, Rbody, is connected from the body node to the source in modeling devices with body-ties i.e. devices in which the body is electrically contacted to the source. If this resistance is left out, the model represents a floating body device.

It should be noted that the kink effect [50] associated with SOI transistors is considered a second order effect for the purpose of SE modeling and is not included in this model. Two justifications for this are 1) the model was developed for devices with body-ties which effectively eliminate the kink in the voltage ranges of interest, and 2) even in the floating body devices, the device terminal voltages during the upset are not in the range where the kink is seen to occur for the devices studied. A shunt resistance may be included between the internal drain and source nodes to model any leakage in the OFF device although it is negligible for devices of reasonable quality and does not effect the outcome of SEU simulations.

3.3.2 Determination of Model Parameters.

As previously stated, the lumped parameter model can be divided into the two device models, the body resistance, and the leakage resistance. The parameter values associated with each of the sections are determined empirically based on a set of measurements performed on the device being modeled (or a representative test device from which the parameters can be scaled). Some of the parameters may be calculated from geometry, doping profiles, and bias conditions. In this subsection, the emphasis of the parameterization is placed on those parameters which have been identified as being most important for SE modeling. Consequently, characterization of the bipolar gain characteristics (including the body tie effects) is the area of concentration in this subsection.

3.3.2.1 MOSFET Parameters. The model parameters associated with the MOSFET model are determined by standard MOS parameter extraction techniques using devices with the body tied to the source to keep the parasitic bipolar from becoming active. I-V and C-V characteristics are measured and the SPICE MOSFET model parameters are optimized using computer optimization techniques to match the measured data. At the time of this work, this capability did not exist at Vanderbilt but was being developed. Most of the MOSFET model parameters used in the simulations where extracted at and provided by the manufacturer of the devices, Texas Instruments, as was all of the data on measured device characteristics used to determine the bipolar model parameters and body resistance values. Overlap capacitances were calculated using overlap areas and oxide thickness information provided by TI.

The bulk MOSFET model in TRIGSPICE handles the MOSFET characteristics well for the purpose of SE effect modeling with one important difference which must be accounted for. The junction areas (used to calculate area dependent saturation currents and capacitances) for these

fully bottomed junction structures is the vertical junction area shown in Figure 17 and not the area of the bottom of the drain or source. These values must be specified in the model parameters and are calculated by multiplying the MOS width by the epi (active) layer thickness. The sheet resistance parameters should be set to zero so that the drain and source resistances are included properly as previously discussed. In addition, the saturation current parameter (JS or IS) should be set to zero in order to deactivate the MOS model junction diodes.

3.3.2.2 BJT Parameters. The bipolar parameters may be determined by standard extraction and optimization techniques to obtain a complete set of values for the SPICE BJT model. For the purpose of this work, the set of measurements are described from which the gain related parameters most significant to single event effects modeling are obtained. Parameters for the bipolar model are determined from the measured device characteristics for the forward active mode [65] as described in [66]. The bipolar gain characteristics are measured on devices which do not have the body connected to the source but which do have an externally accessible body terminal which can be used to control the body potential as shown in Figure 19. The source is

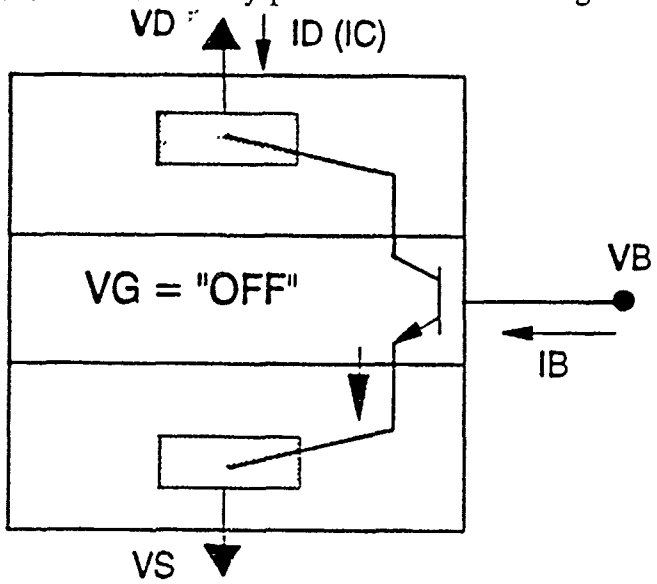


Figure 19. Configuration for gain measurement.

grounded and the gate is offset from the body by 5 volts (+5 for a p-channel, -5 for an n-channel) to keep the body-gate potential constant and bias the MOS OFF. The drain (collector) current and the body (base) currents are measured as a function of the body voltage (VB) for a set of drain bias voltages. The drain voltages for the n-channel device should range from the low supply voltage (VSS) or a voltage just above that necessary to ensure that the body-drain junction remains reverse biased during the measurement, to the high supply voltage associated with the SRAM (VDD), and from zero to -VDD for the p-channel device. The body voltage is swept from a value less than that necessary to forward bias the body-source junction, through a range sufficient to "turn on" the bipolar, and to a voltage such that high injection characteristics are

observed and the bipolar gain is seen to decrease [66-67]. This range is typically zero to 1 volt. The bipolar gain (linear scale), β (β=IDD/IBB, IDD=drain (collector) current, IBB=body (base) current) and the body and drain currents (log scale) are plotted as a function of the body voltage. The initial model parameter values are chosen from these plots as described in [66] and are adjusted to fit the gain characteristics in an iterative manner. An example of simulated gain curves typical of those measured and simulated are shown in Figure 20. These gain characteristics are typical of lateral bipolar transistors [68]. The curves shown are for an n-channel device, and the Y axis (β) has an arbitrary scale due to proprietary considerations.

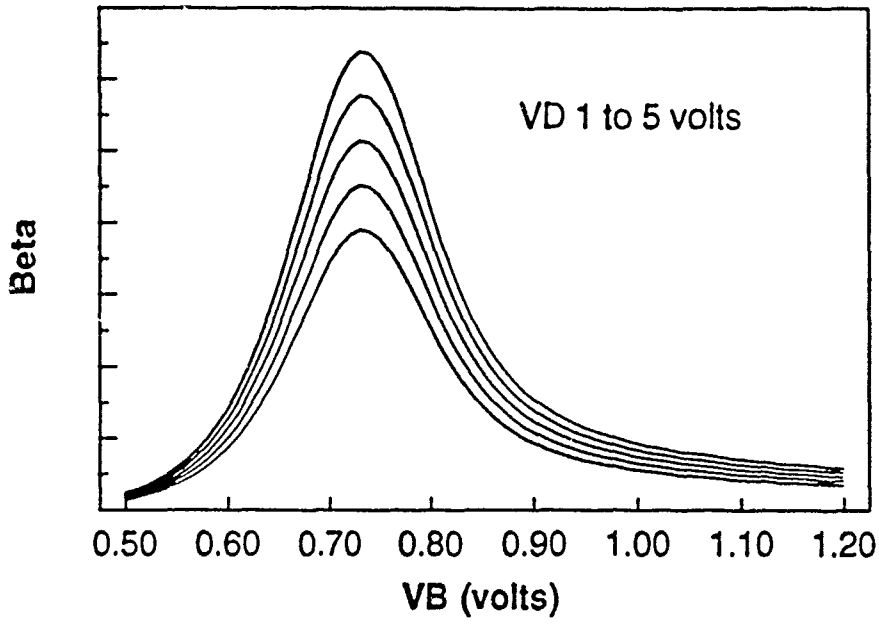


Figure 20. Simulated bipolar gain characteristics.

The dependence of the gain on the drain bias is result of the Early effect [69]. In the measured curves, an increase in bias dependence is seen at the higher collector bias due to the onset of breakdown. Breakdown is not included in this model. For the body-tied-to-source devices, the drain bias dependence of the gain due to the Early and breakdown effects is not significant for the purpose of this work. As will be shown in later, the bias voltages of the bipolar during the single-event cause the bipolar to operate in a region of the gain curves where the dynamic range of the gain is small due to the body resistance. This is not the case for devices with floating bodies, and the precise modeling of this bias dependence is the subject of ongoing work. For the devices modeled in this work, the characteristics measured at the drain bias corresponding the high supply voltage of the SRAM circuit are used. This provides a conservative or "worst case" model in SEU simulations.

The saturation current parameters (IS and ISE) and high current roll-off parameter (IKF), influence the general shape of the gain curve. IS can be approximated by examining the body current at VB=0 [66], and tends to effect the "rise" and position of the peak. ISE and ISC along with NE and NC determine non-ideal junction currents. ISE and NE are predominant since it is the base-emitter junction which is forward biased. These also effect shape of the gain curve. IKF is the high current roll-off parameter. This models the decrease in gain at high currents due to high injection and other non-ideal effects. This parameter can be approximated by examining the "roll-off" in collector current with constant base current as the base voltage is increased. The forward gain parameter (BF) and non-ideality factor (NE) adjust the peak magnitude along with the forward early voltage (VAF) which effects the peak and may be used in matching the bias dependence of the gain. Junction capacitances in the bipolar model are set to zero since they are included in the MOS portion of the macro model. In addition, the forward transit time parameter, TF, which determines the diffusion capacitance should be set to zero. This is because of the frequency limitations associated with the validity of the diffusion capacitance model [70]. Use of a real TF value will cause a non-physical diffusion capacitance value to be used by SPICE, and leads to erroneously high values for predicted critical charge. The diffusion capacitance value is not real because of the high frequency of the single-event current pulse. As will be discussed, the current pulse has a rise time on the order of 5 ps. This corresponds to a frequency of 200 GHz which is well is excess of the validity range of the model. The diffusion capacitance should be more important in dose rate modeling and the implementation of a more complete frequency dependent model capable of modeling high frequency characteristics is another area of ongoing work. The reverse active mode parameter values are approximately the same as the corresponding forward active mode parameter values due to the symmetry of the devices. However, it is the forward active mode which is important in the SE model.

3.3.2.3 Body and Leakage Resistances. The body resistance can be calculated from the device geometry and the sheet resistance of the active region material, or may be measured. To measure this resistance, a device with both the body contacted to the source and the external body terminal, as shown in Figure 21, is used. The gate of the MOSFET is biased OFF as in the case of the bipolar measurement. The I-V characteristics at values of VB less than that necessary to forward bias the body-source junction are used to calculate the body resistance at the desired drain bias using Ohm's law. This may be corrupted by junction leakage current at the body-source junction, but for reasonable quality devices the leakage is orders of magnitude below the current through the body resistor. The resistance value used in the SEU simulations is that measured with a drain bias corresponding to that of the OFF n-channel device in the SRAM circuit. The drain bias will affect the width of the body-drain junction depletion region and thus the effective width of the body resistor. During a single-event upset, the drain bias changes and thus this resistance is in fact dynamic. For the devices studied, the percent variation in this resistance due to this effect is small, and is not a significant factor in the SEU simulations.

After bipolar parameters are fit to the measured characteristics, and the body resistance is determined, the net gain (including the body-tie effect on the gain) is matched to the gain characteristics measured on the device with the body tied to the source. The final simulated gain

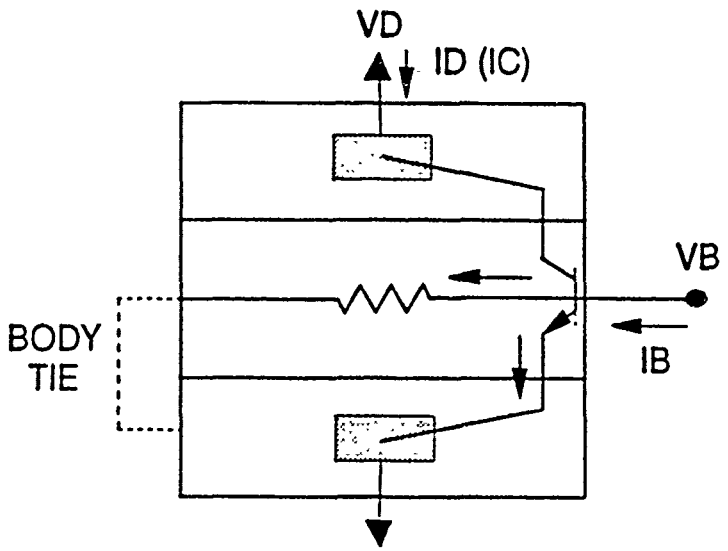


Figure 21. Configuration for measurement of body resistance.

curves corresponding to those of Figure 20 and including the body resistance are shown in Figure 22.

The leakage resistance value is chosen to model the abrupt increase in gain which is seen to occur in leaky devices at low values of VB. A few of the devices studied early in this research showed such characteristics, but the majority of the devices where of better quality and did not. This resistance may be included for completeness, however it does not affect the results of SEU simulations.

3.3.2.4 Single-Event Current Pulse.

The current pulse in Figure 23, Iseu, is used to model the photocurrent which is induced at the body-drain junction by the ion. The pulse which is used in the simulations is a double exponential, that is exponential rise and exponential fall, with a very fast rise time constant (5 picoseconds) and a somewhat longer fall time constant (200 picoseconds). The exact values are not particularly important providing that the time constants are chosen such that the time over which the charge is deposited by the pulse is much less than the response time of the circuit. This pulse has been used in other SEU simulations with good results [71]. Figure 24 shows the time profile of this pulse with a maximum amplitude of one.

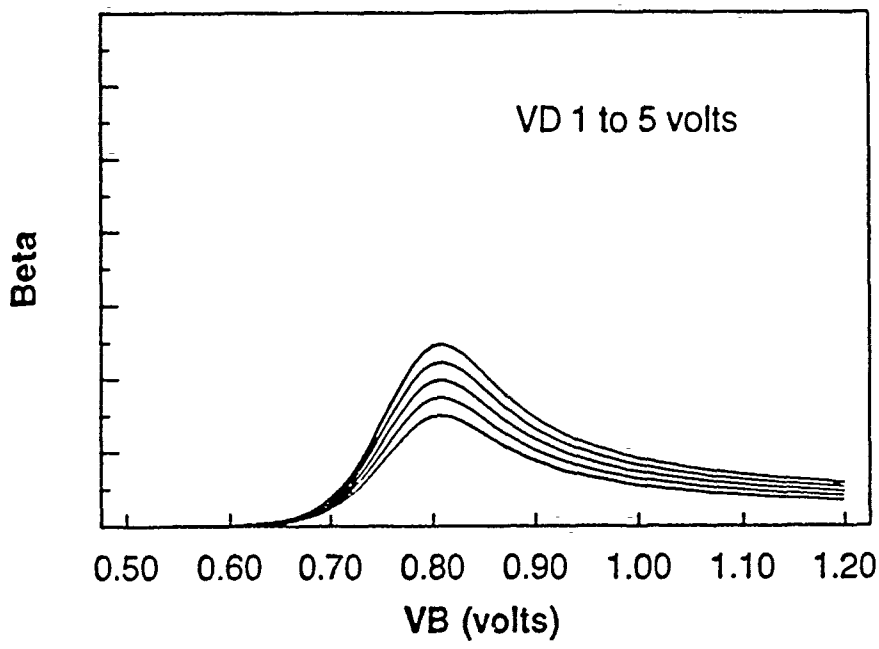


Figure 22. Simulated bipolar gain characteristics including the body-tie effect.

3.4 SINGLE-EVENT UPSET SIMULATIONS.

The SOI model developed in the previous subsections is used in SEU simulations to predict critical charge values for four Texas Instrument SRAMs. In this subsection, the circuit used in these simulations is described. Simulated critical charge values are presented and compared to measured experimental values. Finally, the effects of various device model parameters of interest on the simulation results is discussed.

3.4.1 SRAM Circuit Used in SEU Simulations.

The SRAM circuit used for the SEU simulations is shown in Figure 25 for an n-channel hit. This work concentrated on n-channel hits, although the approach is applicable to p-channel hits also. The circuit is a standard SRAM cell composed of two cross coupled inverters and two access transistors.

The capacitances shown are used to model cell parasitic capacitances which are lumped into C1, C2, and C12. The SOI device model with the single-event current pulse is used as the OFF n-channel device which is hit. The current pulse represents the ion induced photo current which provides base current for the parasitic bipolar and appears from the drain to the body of the OFF

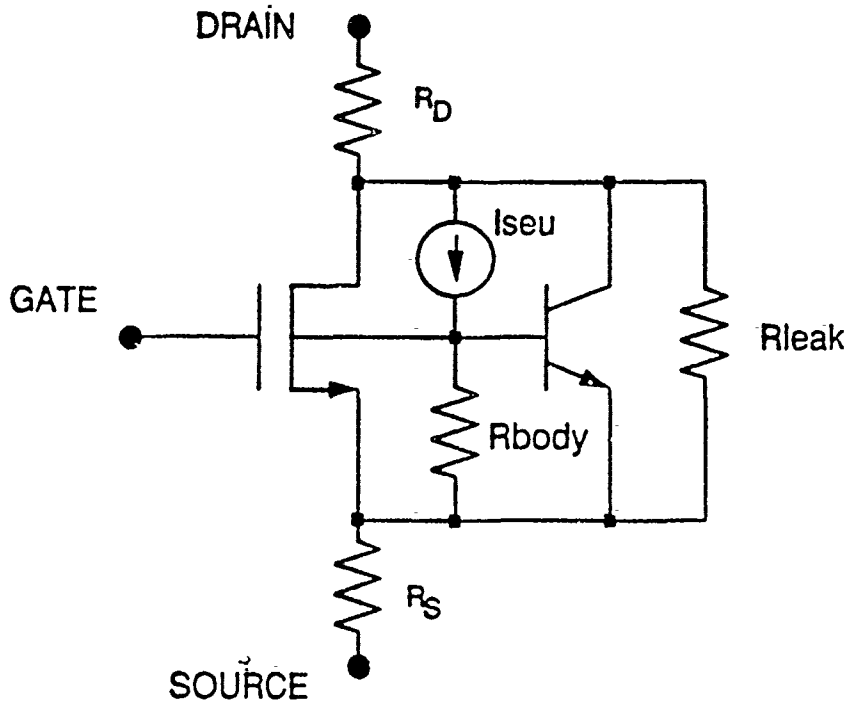


Figure 23. N-channel device model with single-event pulse.

n-channel device for an n-channel hit, and from the body to the drain of the OFF p-channel device for a p-channel hit.

Standard bulk MOSFET models are used for the other transistors in the circuit for the sake of speed and simplicity. This is a reasonable approach since these devices have body ties which suppress the floating body effects. The junctions areas of all devices are specified as the vertical junction areas so that the proper junction capacitances are used in the simulations.

3.4.2 Upset Simulations and Calculations of Critical Charge.

In order to determine the critical charge, the magnitude of the SE current pulse is adjusted until the cell upsets.

The total current which destabilizes the information node in closest proximity to the hit is the current through the drain resistor of the hit device. As can be seen in Figure 25, this is the sum of 1) the photo current (Iseu), 2) the bipolar collector current, and 3) any contribution from the MOSFET which becomes significant as the OFF device turns ON. These three components are shown in Figure 26 along with the total current during a typical upset simulation. The curve labeled ION represents the normalized ion induced photocurrent modeled by the single-event

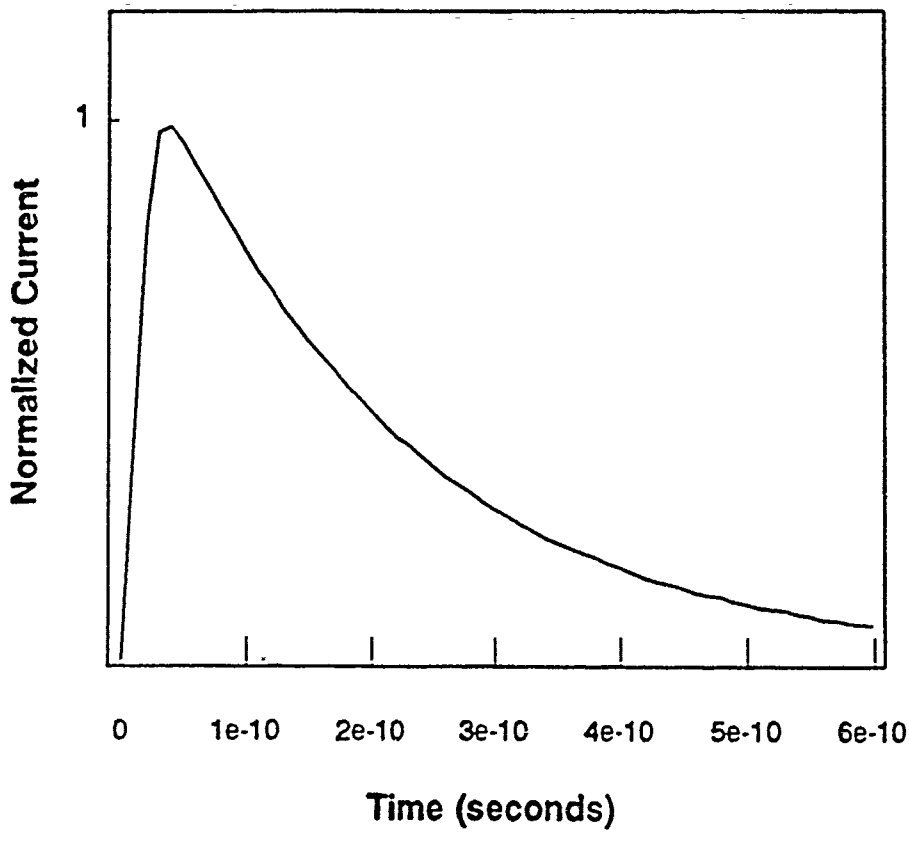


Figure 24. Normalized magnitude time profile of the single-event current pulse.

current pulse. The other curves are also normalized to the ion current. It can be seen that the bipolar collector for this typical case, adds a significant contribution to the total. The charge which is added to or removed from the node is the integral of the total current. This is the charge that the hit device must draw from the high node (or add to the low node in the case of a p-channel hit) to upset the SRAM. Herein lies a subtle distinction in the definition of critical charge for SOI devices. The critical charge is a circuit parameter which corresponds to the amount of charge which must be added to or removed from the information node to cause the SRAM to change state. In a bulk CMOS process, this corresponds directly to the induced by ionization and collected at the drain node due to funneling. Thus there is a one to one correspondence between collected and critical charge in bulk devices. By knowing the characteristics of the ion used to induce an upset, the charge deposited and collected can be determined, and this is the critical charge. In SOI devices however, the ion-induced charge which is collected is not the same as the total charge which is added to or removed from the information node due to the contribution of the parasitic bipolar. In fact, for devices with high bipolar gains, the charge deposited by the ion (collected charge) and the critical charge may vary greatly. If the bipolar contribution is not accounted for, simulations will predict that an ion having an LET capable of inducing the charge calculated as the integral of the total current in

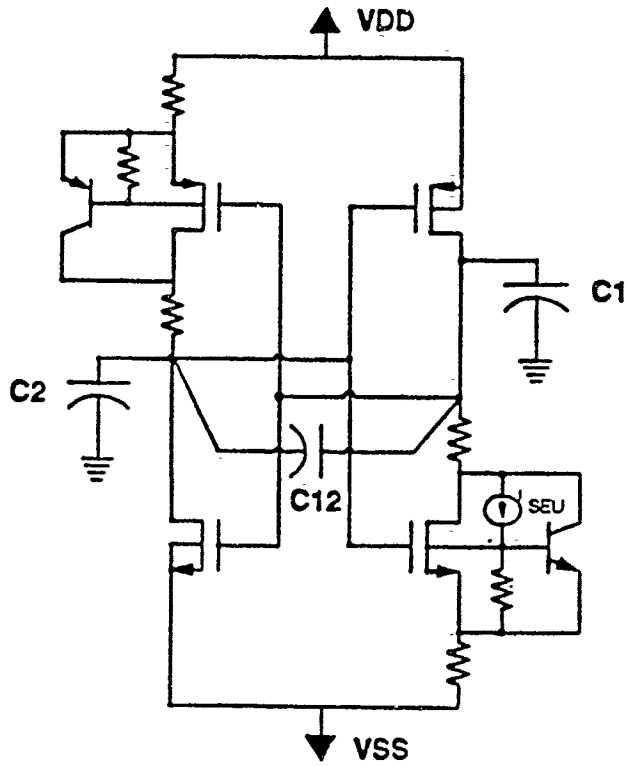


Figure 25. The complete SRAM used in the SEU simulations.

Figure 26, is necessary to upset the cell. This is the true amount of charge which must be added to or removed from the information node to upset the cell. With the bipolar contribution included, simulations predict that an ion having an LET sufficient to induce the charge corresponding to the area under the ion current curve in Figure 26 is capable of causing an upset. Because of the bipolar amplification, the ion needs only to induce an amount of charge such that the ion charge (area under the ion current curve) and bipolar charge contributions (area under the bipolar sum to the total charge necessary to upset the cell (area under the total current curve). In presentation of the simulation results, the charge calculated as the integral of the ion current, that is the charge deposited and collected, is reported as the critical charge. This is because it is this value which is the externally measurable parameter in SEU experiments using ion bombardment. This allows the simulation results to be compared to experimental results.

The upset is defined as the point at which the SRAM information node voltages cross. These voltages, high going low and low going high during the upset, are shown in Figure 27. In addition, the body voltage of the hit device, or base voltage of the bipolar, is shown. The bipolar "turns on" and the base-emitter voltage remains fairly constant during the upset after which the bipolar "turns off". Because the drain resistance is so low, the high to low voltage is the bipolar collector bias during the upset. Thus, the bias is dynamic and the non constant bipolar gain must be included by properly modeling the shape of the gain curves.

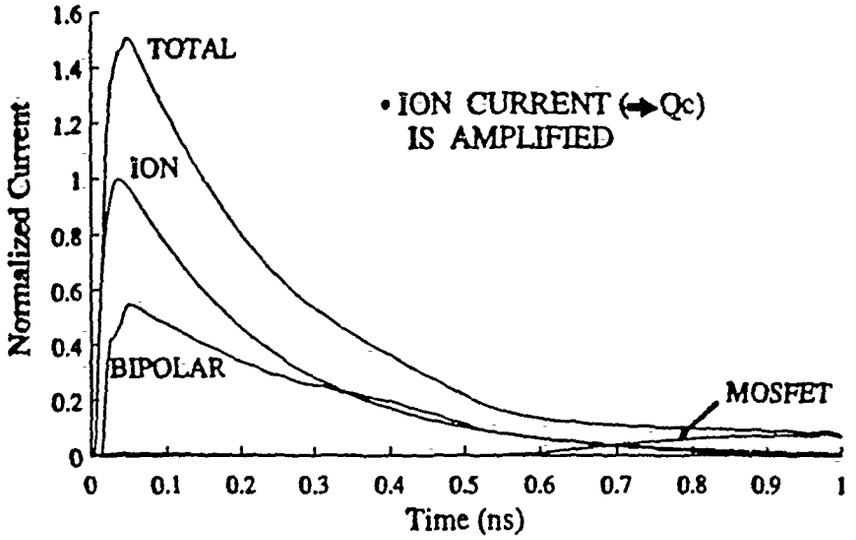


Figure 26. Model currents during the upset.

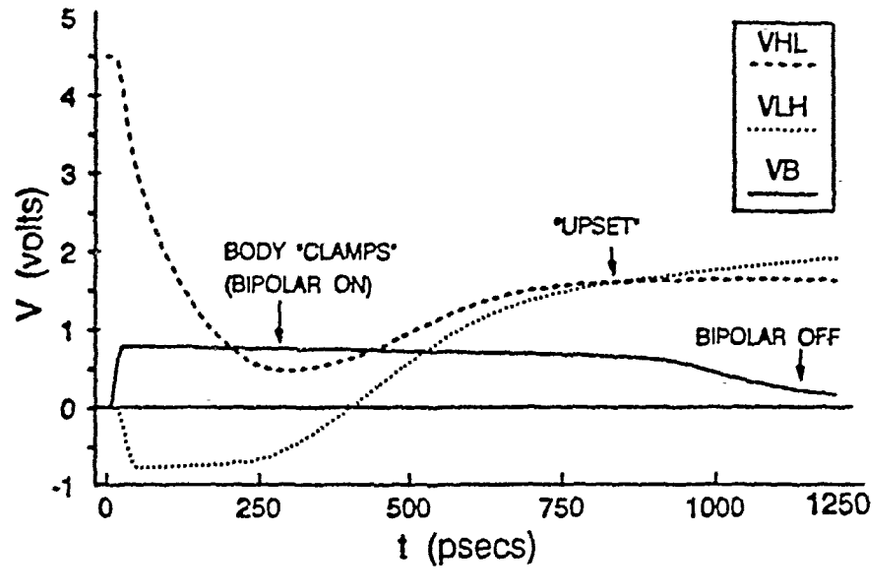


Figure 27. Node voltages of interest during the single-event upset.

3.4.3 Effect of Bipolar Gain Characteristics.

Table 6 shows simulation results using constant gain values and using the bias dependent gains. The constant values used correspond to the peak of the measured value for each device respectively. In each case, the critical charge values predicted using constant gain are lower than those which are predicted using the true gain characteristics and those measured experimentally. The behavior of the gain characteristics during the upset can be determined by using the collector and base voltages during the upset from Figure 27 and the corresponding gain characteristics from Figure 20,i.e. a gain "operating line" can be determined during the upset. The body resistance has the effect of "pinning down" the net gain (adding a component to the measured base current via the current through the body resistance to the tie). Thus, for these devices with body ties, the dynamic range of the gain is fairly low during the upset. From this observation, it is evident that a shift of the peak toward the potential at which the body is held during the upset would increase the gain during upset and decrease the predicted critical charge.

Table 6. Effect of constant gain compared to bias dependent gain.

SRAM Design	Q_c	
	Variable Beta	Constant Beta
SRAM 1	0.19 pC (peak beta = 1.4)	0.16 pC (beta = 1.4)
SRAM 2	0.24 pC (peak beta = 1.4)	0.14 pC (beta = 1.4)
SRAM 3	0.29 pC (peak beta = 1.8)	0.21 pC (beta = 1.8)

This was found to be the case in repeated simulations. In contrast, adjusting the peak gain value has little effect on the results since the gain during the upset does not reach the range of the peak for these devices, but is controlled by the bias voltages and body resistances. Of course, very large changes in the peak will cause changes even in the range of bias during the upset, but reasonable changes (on the order of the 10 to 100 percent) made very little difference in results. It should be noted that the gain of the devices studied was very small compared to typical bipolars, and devices with higher parasitic gains would be more sensitive to these percentage changes. Bipolar charge enhancement should be expected to be more pronounced in floating body

devices since there is no body to source current via a body tie. Because of this, the gain can be expected to reach the range of the peak value at the bias voltages present during upset, and to have a higher dynamic range. In addition, because there is no RC path to discharge the body node, all of the injected charge must be removed from the body as bipolar current (or by recombination).

3.4.4 Effect of Body and Leakage Resistances.

The effect of the body resistance value on the predicted critical charge has been investigated through repeated simulations varying the vales of Rbody each time. The maximum value of the resistance used corresponds to that measured for the device being simulated. This is the resistance of the entire non-depleted body region measured across the device width as previously described. This is also the maximum resistance that can exist between any hit location and the body tie.

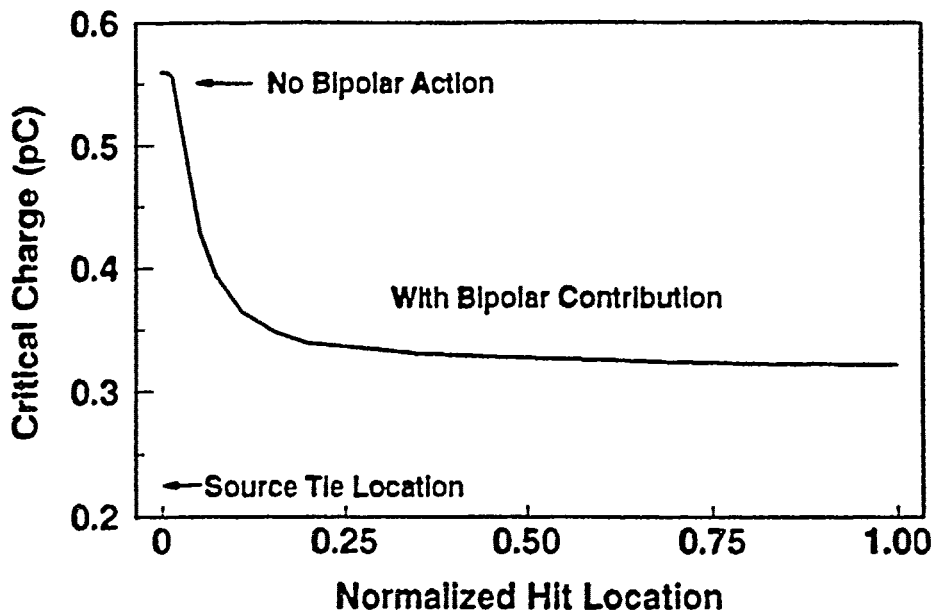


Figure 28. Predicted critical charge as a function of hit location.

Results of such simulations are shown in Figure 28. The figure shows simulated critical charge values vs. the normalized hit location. The normalized hit location corresponds to the ratio of the distance of the hit from the body tie (measured along the gate width axis) to the total gate width. Implicit in this simulation is the assumption that the resistance is constant along the width of the body (uniform doping). As can be seen by the these results, the body tie makes very little difference until the hit gets very close to the tie (less than 15% of the device width in this case).

Thus the body tie does not eliminate the bipolar enhancement of the ion-induced photocurrent. The body tie does decrease the area of the device which is vulnerable to ions corresponding to the lower critical charge level but only by a small percentage.

3.4.5 Comparison of Experimental and Simulation Results.

Single event upset levels were measured for four TI SRAMS. The SEU tests were conducted at the Brookhaven National Laboratories Tandem Van de Graff accelerator facility. JPL beam control and exposure equipment [72] was used to monitor beam fluence and incidence angle. The SRAMS where irradiated with 149 MeV Fe, 260 Mev Br, and 300 MeV Au at various incidence angles ranging from 0 to 70 degrees. The SRAMS were in standby mode during irradiation with a stored checkerboard pattern. Supply voltages of VDD=4.5 volts and Vbb=0 volts (substrate bias) were used. The memories were tested using a Mosaid portable memory tester. Both "1" and "0" errors were observed with no favored state. Multiple samples of each cell design were tested. Critical charge values were calculated from the threshold linear energy transfer (LET) values taken as the LET values at 25% of the saturated cross section. The calculation of the critical charge from the LET makes the assumption that only charge deposited in the active layer contributes to the upset. Table 7 shows the critical charge levels predicted by the simulations compared to those measured for the four SRAMS. The range of experimental data corresponds to the range of spread in the LET data. The results provided by the simulations are within 7.5 percent of the experimental values for the designs simulated in this study.

Table 7. Simulated and experimental critical charge results.

SRAM Design	Simulated Qc	Experimental Qc
SRAM 1	0.19 pC	0.20 pC
SRAM 2	0.24 pC	0.26 pC
SRAM 3	0.29 pC	0.30 pC
SRAM 4	0.046 pC	0.048 pC

3.5 DISTRIBUTED PARAMETER MODEL.

This subsection presents a distributed parameter version of the SOI model. The lumped parameter model presented in the preceding subsections does not provide for devices with multiple body ties as opposed to single body tied to source devices (SBTS). In addition, the distributed parameter model allows for more accurate representation of the distributed resistances and capacitances in the body region. This is useful for some of analyses regarding sensitivity to various parameters. The use of a distributed parameter model in SEU simulations yields results almost identical to the results obtained using the lumped parameter model for the same conditions, while providing the capability for multiple double body tie configurations and additional parameter sensitivity analysis. Because the model uses multiple devices to model a single device there is a significant increase in complexity execution time, and memory requirements. A description of model parameterization is included.

3.5.1 Distributed Model Implementation.

In order to allow comparison between SBTS and DBTS (double body tied to source) configurations, as well as doing certain parameter sensitivity analysis such as hit location, it is helpful to distribute the parameters among a number of parallel devices configured such that they model the performance of a single device. It is necessary to distribute both the MOSFET and bipolar devices as well as body resistance in order to accurately model voltage dependent capacitances and analyze hit location sensitivity.

In this model, the same set of parameters as are used in the lumped model are necessary. The distributed model shown in Figure 29, consists of multiple parallel lumped parameter models with the area dependent parameters and the body resistance distributed among the devices appropriately. Figure 29 shows the model divided into N lumped parameter models. The choice of the number of devices is somewhat arbitrary, and the accuracy and sensitivity to device number is discussed. The only constraint is that there be an odd number of devices (even number of distributed body resistors) to maintain symmetry.

The parameters which depend on area must be divided by the number of devices. These include the MOSFET drain and source areas (AD and AS), and the device width (W). If area scaled parameters are used, changing the junction areas and device width will adjust the area dependent parameters accordingly. Because the leakage resistance is in parallel with the devices (drain to source), it can be left as a single resistor and need not be distributed. As previously shown, it has no significant effect on the SEU simulation results The extrinsic drain and source resistances are also left as a single resistor since in the distributed model they would also appear in parallel. When the DC characterization measurements are made, only some portion of the device becomes active due to the high resistivity of the body material [73]. This decreases the forward bias on the body-source junction with increasing distance from the body contact. Measurements have indicated that it is a relatively small portion of the device which becomes active. Unfortunately however, we have not been able to quantify this as yet. For the case of a single event, it is

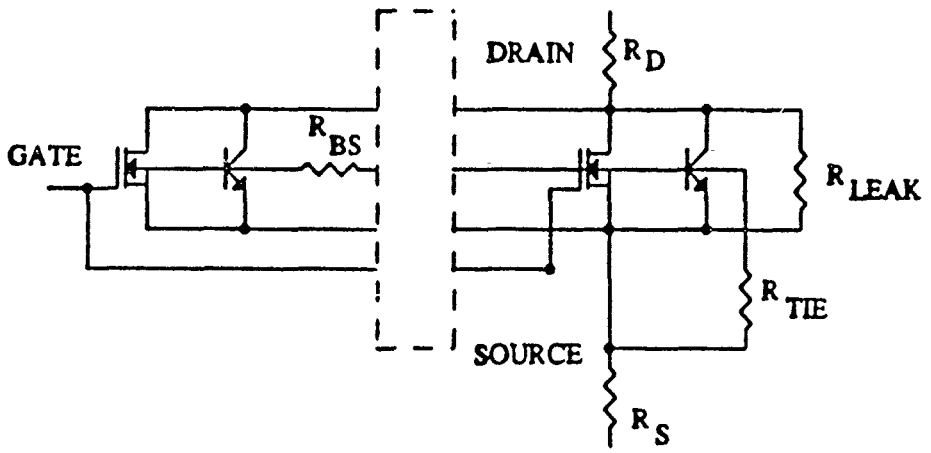


Figure 29. N-channel distributed parameter model.

reasonable to assume that similar characteristics would exist because on the small ion track diameter [74], and thus the bipolar parameters remain the same for the distributed model. In order to apply this modeling approach to gamma dot radiation analysis, where the entire body region is injected with charge, it will be necessary to quantify how much of the device becomes active during the DC measurements in order to accurately choose the number of devices to use in the distributed model.

3.5.2 Parameter Sensitivity.

3.5.2.1 Number of Devices. As previously stated, an arbitrary number of devices was chosen at the beginning of the distributed parameter model development. In order to determine the effect of the number of devices on the model, simulations were run for models divided into 3, 5, 9, 17, and 25 parallel sets of the MOSFET/Bipolar combination with the parameters distributed as discussed. The results, shown in Figure 30, show that increasing the number of devices has very little effect on the critical charge, and that both the designs simulated show the same insensitivities to this number. Additionally, the simulation run time increases by a factor of 6 in going from 3 devices to 25 devices. Based on these results, three devices seems provide to be quite sufficient accuracy while minimizing CPU time and memory, and allowing for both SBTS and DBTS configurations.

3.5.2.2 Hit Location. Hit location analysis shows the worst case hit for the SBTS to be farthest away from the body tie for the three device model. As the number of devices is increased, there is less resistance between any two adjacent bipolar transistors in the model. The decreasing

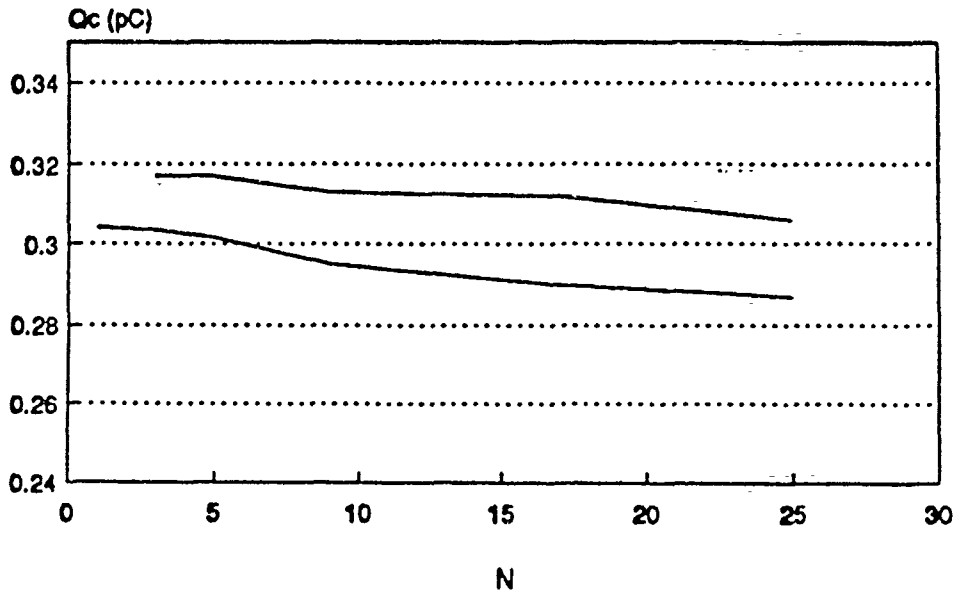


Figure 30. Critical charge as a function of the number of distributed devices.

resistance allows the devices adjacent to the hit device to turn on to a larger extent as the number of devices is increased. For the five device case, moving the hit one device in from the device farthest from the tie causes an insignificant change in the results. Using nine devices, the bipolar where the hit occurs along with the bipolar(s) immediately adjacent to the hit device, are the primary contributors to the upset current (with the worst case being one in from the end). However, the magnitude of the current contribution from the adjacent device(s) is negligible compared to that of the hit device. Figure 31 shows the individual bipolar transistor collector currents of the hit device and the immediately adjacent devices for a nine device model during a single event upset. For both the SBTS and DBTS configurations, it can be seen that only the device at which the hit occurs contributes significant current to the upset. As the number of devices is increased still more, this same trend is observed, that is that the devices adjacent to the hit device contribute to the total upset current. The net effect is the same however, since the process is current limited by the ion induced current. This limits the total available base current. It is the sum of the collector currents which determines the upset level. This sum is virtually independent of device number since the total base current is the same in each case. There is only a very slight difference in the predicted worst case critical charge as the hit location is moved from device to device (until the hit is very close to the tie) for the models with larger number of devices. This is due to the difference in the distributed resistance and capacitance between the hit and the tie. The difference does not become significant until this resistance and capacitance correspond to the hit very close to the tie. In the case of the smaller models (3 or 5 devices) there is a more abrupt difference because as the hit is moved closer to the tie, the change in resistance for each step is larger.

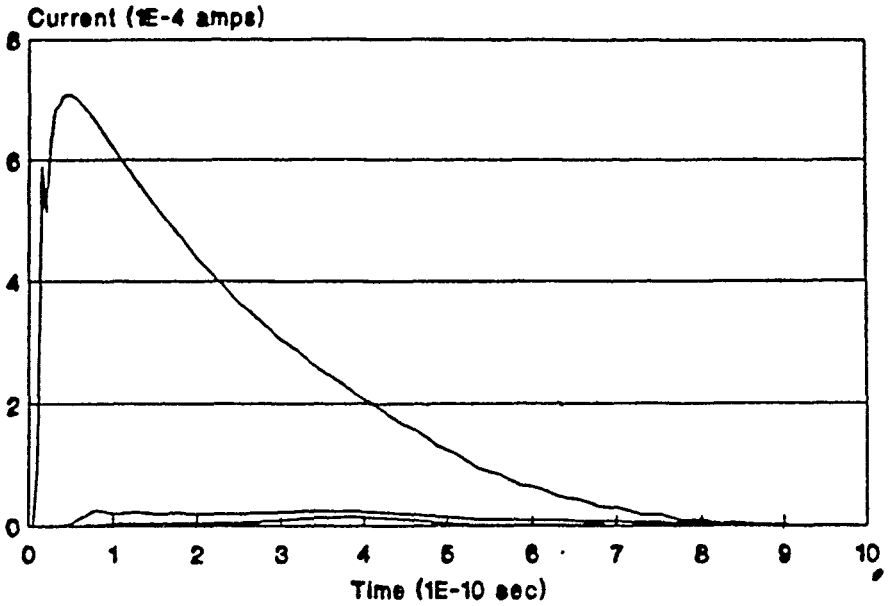


Figure 31. Bipolar collector currents for the 9-device model.

While a larger number of devices gives better resolution, it is of little value since the critical charge remains practically constant until the hit is very close to the tie. For smaller width devices in which the transition region (i.e. moving from bipolar enhancement to no bipolar enhancement) corresponds to the device width, this may be more important. In the case of the DBTS configured device model, the worst case hit location is found to be the center (farthest from both body ties) independent of the number of models. Again, the critical charge remains virtually constant until the hit is close to one of the ties. Thus, for both SBTS and DBTS devices modeled, all of the body region which is more than a few thousand ohms from the tie is vulnerable and yields the same critical charge value.

3.5.3 Body Resistance.

Increasing the overall body resistance by ten percent only makes the SBTS device two percent softer while increasing peak β by fourteen percent makes the device only about four percent softer. An increase of twenty percent in both body resistance and bipolar gain makes the SBTS device six percent softer. This indicates that the critical charge is relatively insensitive to these parameters which is consistent with results presented for simulations using the lumped parameter model.

3.5.4 Results.

Using this model and the parameters for SRAM 2 design, single event simulations show the same results as the lumped parameter model for the SBTS configuration. Simulations on the DBTS configuration show a eight percent increase in critical charge, while the experimental data shows about a fifteen percent difference. This difference may be due to the values of body resistance used, differences in the bipolar characteristics which are not accounted for, or to the curve fit to the small number of experimental data points. The distributed model is of limited importance in SEU simulations, however, it should be a very useful modeling approach for dose rate modeling.

3.6 CONCLUSIONS.

A simple model for prediction of single-event vulnerability of CMOS/SOI transistors and circuits has been developed and shows excellent agreement with SEU experimental data. The model can be easily implemented in SPICE (as done here) or SPICE-like circuit simulators.

It has been shown that the parasitic bipolar structure may significantly increase the single-event vulnerability of SOI devices. Critical charge levels are sensitive to the value of body resistance and the gain profile of the parasitic lateral bipolar structure. This suggests that the effect of the lateral bipolar structure will become more pronounced as smaller feature sizes and better materials are used [75]. In addition it gives an indication of single-event vulnerability vs. feature size for a given SOI process. While body ties may reduce or eliminate parasitic bipolar gain during normal operation, they do not eliminate it during single events. It may be possible to reduce or eliminate the effect of the parasitic bipolar structure by use of techniques which degrade bipolar gain such as those used in bulk MOS processes [76-77], or by going to thinner active layers i.e. fully depleted devices.

3.7 FUTURE WORK.

It should be noted that this model has been specifically developed to model SE effects on non-fully depleted SOI devices with fully bottomed junctions and the body contacted to the source. It does not necessarily encompass all aspects of normal device operating characteristics. No provisions are made for the "kink" effect associated with floating body devices or for back gate bias conditions which become increasingly important as the device thicknesses decrease (fully depleted structures). These are believed to be second order effects for the purpose of SEU modeling of the particular devices discussed here. The back gate bias is known to effect the front gate threshold voltage [55]. To account for this in the model, the MOSFET model threshold voltage may be adjusted to the reflect the back gate bias condition. These effects are the subject of ongoing modeling efforts in order to generalize this modeling approach to other isolation structure devices. Recent advances in materials and fabrication capabilities have made thin film SOI devices attractive due to the advantages associated with the fully depleted structures [37,59,61,78]. The modeling of single-event effects on these devices is of particular interest. In

addition to generalization of the single-event model to other particular device configurations or operating modes, other areas of ongoing work include the addition of side and back channel effects in order to model transient (dose rate) and total dose radiation effects on SOI devices and circuits, and error rate predictions based on statistical analyses results of SEU simulations such as those presented in this work.

SECTION 4

THE SCALING OF SINGLE-EVENT EFFECTS

4.1 INTRODUCTION.

When the analytical study of single-event effects began, it was a different world. Device feature sizes were 7 μm, or larger, and many of the "exotic" technologies showing promise today, including trenched DRAM technologies and insulated technologies, were not even a gleam in designers' eyes. Charge collection by IC devices from ion tracks had not been accurately described analytically; field funneling [62, 79, 80] had not been "discovered". Still, single-event upset had been predicted as a "fundamental limit" on IC scaling [81], and single-event upsets had been "discovered" in space-borne ICs [82]. Some fundamental work on the scaling of devices in future commercial technologies had been conducted [83-87]. The engineering community had formed some habits in viewing scaling, predominantly regarding the acceptance of "constant-field" scaling [87].

The first works on the scaling of single-event effects [88, 89] were based on the acceptance of constant-field scaling for future devices and on a "figure of merit" [90] for assessing the vulnerability of ICs, given information on their feature size and total sensitive area; funneling was "patched" onto these models as an estimated extension in sensitive volume.

This section is not intended to criticize earlier work -- that work was based on the best knowledge available at the time -- but it is intended to establish and project the consequences of *assumptions* on which that work was based that have not proven to be characteristic of today's devices and those being developed for tomorrow, and also to point out areas in which long-terms habits of viewing devices and their responses are not appropriate for present and projected future ICs.

Other than raising hopefully valid questions, this work is incomplete. It does not end with analytical expressions for the scaled vulnerability of ICs to single events. In this way, it is an interim report on a work still in progress. Some roadblocks have been encountered. Most important is a deficiency in publicly available literature on the actual rules used to design and to scale present devices; most of this information is highly proprietary in the present highly competitive semiconductor device world community. Constant field scaling has not been used for some time, and no published work has detailed its successor.

Still, this report describes an *approach* to the problem that may guide those privy to actual scaling rules and provide a basis for future study. The report also provides predicted *trends* for single-event vulnerability, though they are, unfortunately, not quantitative. This section is divided

into four principal parts: Rethinking Definitions, Anticipating Technology Directions, Defining Sensitivity Scaling, and Considering Probable Vulnerabilities.

4.2 RETHINKING DEFINITIONS.

The following is a discussion of the "habits" of thought concerning single-event effects that are inappropriate for some present and future technologies. These include the relationships of collected charge, Q_{coll}, to critical charge, Q_{crit}, and the linear energy transfer, LET, of ions inducing upset, and the relationships between sensitive area, collection volume and collecting volume. The consequences of these relationships, and of possible errors in the use of these relationships in past works, is not addressed, although the basis for addressing these issues during future research is provided in part by recent work due to Langworthy [91].

4.2.1 Upset Threshold Measures.

The charge collected onto a node from ion-induced ionization, Q_{coll}, depends on the characteristics of the impinging ion, including its atomic number and its initial energy, and also on the characteristics of the charge-collecting node and the surrounding region, including their doping levels, carrier mobilities and the deposited energy required to create carrier pairs. Q_{coll} is the result of an interaction between an ion and the *technology* of the IC it hits.

The "critical charge" for single-event upset, Q_{crit}, is defined as the amount of charge differential on a charge-storage node required to initiate a logic-state reversal in the parent IC. This definition is unambiguous in the case of dynamic RAMs [92], where the node "sensitive" to charge collected from ions and the node storing information are collocated. For digital circuits in which information storage is spatially "distributed" and involves regions not vulnerable to charge collection directly from ion tracks, the term Q_{crit} is still used to represent the total integrated charge perturbation associated with upset (such as SRAM cells, latches and combinational logic), although in these circuits, not only the total charge perturbation, Q_{crit}, but also the time profile of charge deposition and transport to information-storage areas actually determines vulnerability to single events. While the existence of time dependencies for single-event upset has been addressed and incorporated into computer simulation analyses of single-event effects [44, 93], these dependencies have not been incorporated into analytical expressions for upset vulnerability, nor into upset rate predictions.

Q_{crit} is a *circuit* characteristic, i.e., differences in circuit design and layout can change the value of Q_{crit} for devices processed in the same technology. It does not depend on characteristics of the impinging ion.

For older technologies and circuits, the criterion for single-event upset could be expressed as: $Q_{coll} = Q_{crit}$. A better criterion, one applicable to all ICs (given the caveats associated with time dependencies) is that Q_{coll} *results in* Q_{crit}. This association incorporates the possibility that the

amount of charge collected from an ion track may interact with junctions and/or devices in ways that amplify or diminish the amount of charge that perturbs charge stored in support of a logic state.

LET, or linear energy transfer, refers to the amount of charge deposited per unit path length of an impinging ion. The critical LET of an IC, refers to the LET of an ion impinging on an IC resulting in single-event upset. There is, of course, a relationship between the critical LET and Q_{coll}, as a portion of the ion track is collected at a "sensitive" node. In advanced circuits, this relationship can be complex for two sets of reasons. First, the amount of charge deposited per unit path length of an ion is not a constant for a given interaction; the LET of an ion *changes* as it passes through material losing energy. During an interaction with an IC, LET can either increase or decrease, depending on the type of ion and its initial energy. Therefore the LET value of an impinging ion, directly measurable only *before* it enters an IC, is not trivially correlated to the energy deposited proximal to sensitive regions. To evaluate the effective critical LET, one must know the precise location and collection length of a sensitive junction, determine the energy deposited in material overlying that collecting region and correct the initial or incident value of LET based on this information. A second factor complicating the straightforward interpretation of critical (incident) LET values obtained from experiment is that identical ions can have identical initial LET values at different initial energies and not produce identical charge tracks within semiconductor materials; the tracks would differ in charge density (and radial charge distribution) [94]. As the charge distribution within a track significantly affects the spatial extent and time duration of induced electric field redistributions within an IC, and these field redistributions are a primary factor determining the amount of deposited charge that will be collected, ions with the same LET do not necessarily result in the same charge being collected at a node. Thus, critical LET alone cannot be unambiguously associated with the charge collected by a sensitive node during a single event.

Despite these factors that make the interpretation of critical LET results difficult and/or imprecise, the initial LET of an ion resulting in single-event upset is the most convenient of experimentally measurable parameter associated with single-event upset. Moreover, it has the tremendous advantage of allowing experimental data to be associated with potential environments, i.e., if an IC is shown experimentally to upset under specific experimental bombardments, the probability that it will upset in actual environments can be obtained by calculating the probability that the circuit will encounter like ions in the actual environment.

By contrast, critical charge calculations can be translated into upset probabilities in real environments only via a complex path. The advantage of critical charge evaluations is that single-event vulnerability is expressed in terms of circuit characteristics, i.e., the upset vulnerability can be *attributed* to circuit characteristics. Thus, critical charge evaluations are crucial to determining changes in layout or circuit design corresponding to decreased upset vulnerability.

Critical charge, collected charge and critical initial LET are each important measures of upset vulnerability, and, while they each related to critical aspects of logic upset, they are different from one another. Each of these measures accesses somewhat different aspects of IC vulnerability

to single events. The important point is that they are neither equivalent nor trivially interrelated. The "habits" incorporated in assuming $Q_{crit} = Q_{coll} = (LET_{crit})/c$ (where c is the thickness of the sensitive node) must be broken, and the instances of their direct or indirect use must be removed from our testing and analysis methods, if we are to accurately understand and evaluate the vulnerability of advanced semiconductor technologies.

4.2.2 Upset Cross-Section Measures.

The distinctions between commonly used measures of upset cross-section are perhaps more subtle than are those for upset threshold. "Sensitive area" refers to the surface projections of volumes in an IC which, when "hit" by an ion, can induce upset. These volumes are device nodes capable of collecting ion-induced charge and electrically transmitting this perturbation to information-storage nodes. Sensitive areas are measured as the areal projections of these vulnerable nodes, i.e., their actual physical dimensions at the IC surface. These representations are unambiguous. A problem arises, however, when these sensitive areas are correlated with the charge they collect. In general, sensitive nodes are surrounded by depletion regions supporting electric fields. If these depletion regions are intercepted by an ion track (as the most often are when an ion impinges on a sensitive area), the fields are perturbed, and charge deposited within portions of this field-perturbed region can be collected onto the sensitive node by funneling. Thus, the collection volume associated with a sensitive node is the volume *surrounding* that node which can respond to an ion interaction by collecting charge, a volume distinct from the collecting volume, which is the actual volume from which charge is collected during a given event, and also distinct from the sensitive volume, which is the volume of the doped region forming the node.

The sensitive node itself is usually degenerately doped, producing what is commonly called a "dead" region in which deposited charge is not collected. For this reason, the sensitive node and the collection volume have no common regions; the collection volume is an annular volume surrounding the sensitive node, the volume supporting electric field gradients during normal circuit operation.

The response of a circuit node to an ion hit is inherently dynamic. The collecting volume is a measure of the dynamic field response resulting in charge collection. Sensitive area and collecting volume are static measures of regions vulnerable to ion interactions, but do not measure the dynamic response of the device to a particular ion hit. The collecting volume (which can depend on the funnel length for charge collection) will in general be different for different ions, or the same ion with different initial energies, impinging on a sensitive area. By contrast, the collection volume and sensitive area are generic measures for a given IC, independent of the ion environment of a given circuit. [It should be noted for completeness that the relationships between these three cross-section measures are also dependent on the time intervals over which an IC is vulnerable. "Integrating" technologies, such as DRAMs and high resistance-load SRAMs, are vulnerable to charge collected by both drift and diffusion, while latched logic with short single-signal write times, such as CMOS SRAMs, are vulnerable only to drift collection (which includes funneling).]

The bottom line is that sensitive area and/or collection volume, which are the commonly used measures of upset cross-section, are imperfect representations of upset cross-section, even for older technologies. An ideal measure would include the dynamic response of device nodes to ion interactions and would therefore be considerably more complex than these static measures; it would, for instance, depend on ion type and initial energy as well as circuit and technology characteristics. No work has addressed this issue.

4.2.3 Applicability of Definitions to New Technologies

For some advanced technologies, the measures for sensitivity and vulnerability to single events described in the preceding subsections simply do not apply. Circuits vulnerable to upset resulting from "ion shunt" charge transport [95], including devices with multilayer structures [96, 97] and those with closely spaced deep nodes [98], upset due to charge transported *through* the single-event track, rather than due to charge collected *from* the ion track. In these cases, critical charge, being a circuit characteristic remains a valid vulnerability measure, but collected charge and critical LET do not have the same relationships to device vulnerability as they do in other technologies.

The ion-shunt mechanism initiates upset by transferring charge already stored in the circuit from one circuit node to another. The charge collected through an ion shunt depends on the relative amounts of charge stored in nodes bridged by the shunt. The charge *within* an ion track is important only in determining its conductivity as a shunt bridging these nodes. Thus, the volume charge density, rather than the linear charge density (LET) becomes the important measure of vulnerability to ion-shunt-induced upset.

The ion-shunt mechanism can also initiate parasitic bipolar action within device multilayers [99, 100], thereby amplifying the charge transferred between devices. The traditional measures of sensitivity and vulnerability do not address the ion shunt mechanism and should therefore not be applied to device containing trenched active regions or multilayers which include sensitive nodes.

4.2.4 Conclusions Regarding Definitions.

Definitions established in the initial years of single-event upset analyses were based on characteristics of technologies produced at that time, and were, even then characterizations of approximate relationships. As technology has advanced and evolved, the "percentage error" between the assumptions couched within these definitions and reality has grown to be non-negligible. Even in the case of applying these definitions to the scaled versions of the technologies on which they were based, significant error can arise. To compound the problem, new technologies, substantially different from any available during "the time of definitions" have been produced and are susceptible to single-event upset via mechanisms entirely distinct from the vulnerability mechanisms of earlier technologies.

Despite the fact that the world of ICs has changed substantially over the last ten years, we have not reexamined our measures for single-event vulnerability and sensitivity in light of these changes. We have continued to rely on a "figure of merit" for device vulnerability based on old definitions, and to use that figure to estimate the vulnerability of parts. We have invested substantial resources into measuring the quantities defined long ago, but none into reconsidering their validity in present times. Most important, we have bet the success of important systems on the accurate evaluation of vulnerability measures that do not necessarily apply to the ICs being evaluated.

4.3 TECHNOLOGY DIRECTIONS.

To consider, albeit qualitatively, vulnerability trends in advanced and future technologies, we must first predict what they will be. The following assumes that four types of technologies will comprise the majority of those used in future space and radiation-hardened applications. The choice of these four technologies is based on the fact that they all offer high density and speed, and relatively low power operation. The technologies considered are: trenched-capacitor DRAMs, resistor-load SRAMs, CMOS SRAMs, and CMOS/SOI-SOS SRAMs. In the following subsections, basic characteristics of these four technologies will be outlined as a basis for a discussion of possible scaling and single-event vulnerability trends in succeeding subsections.

4.3.1 Trenched-Capacitor DRAMs.

Trenched-capacitor DRAMs (TCDRAMs) are a new technology providing the highest information-storage density of any present technology. They also offer promise for future technology evolutions that may make them desirable choices for space systems. The characteristics of trenched-capacitor DRAM ICs relevant to their single-event vulnerability are summarized in Figure 32.

As in other DRAM technologies, TCDRAMs store information on a node that is also a charge collecting node, i.e., the "sensitive" and "information" nodes are collocated in DRAM technologies. They operate by "opening" an access transistor to inject or remove stored charge representing a logic state, then "closing" this transistor to isolate the node and retain information. As charge can leak from these storage nodes, they must be periodically "refreshed".

DRAMs, therefore, can lose (via leakage) or accumulate (via single-event charge deposition) charge during the period between refresh or rewrite cycles. As this period is generally relatively long compared to charge collection times either by drift or diffusion processes, DRAMs can collect more charge from a given hit than comparable SRAM devices. This relatively long "integration time" makes DRAMs vulnerable to upset from the integrated effects of multiple ions each depositing sub-critical amounts of charge. In addition, a single ion track can deposit charge onto multiple DRAM cells, resulting in multiple-bit upset from a single event [101-105]. TCDRAMs are also vulnerable to upset from ion shunts [98].

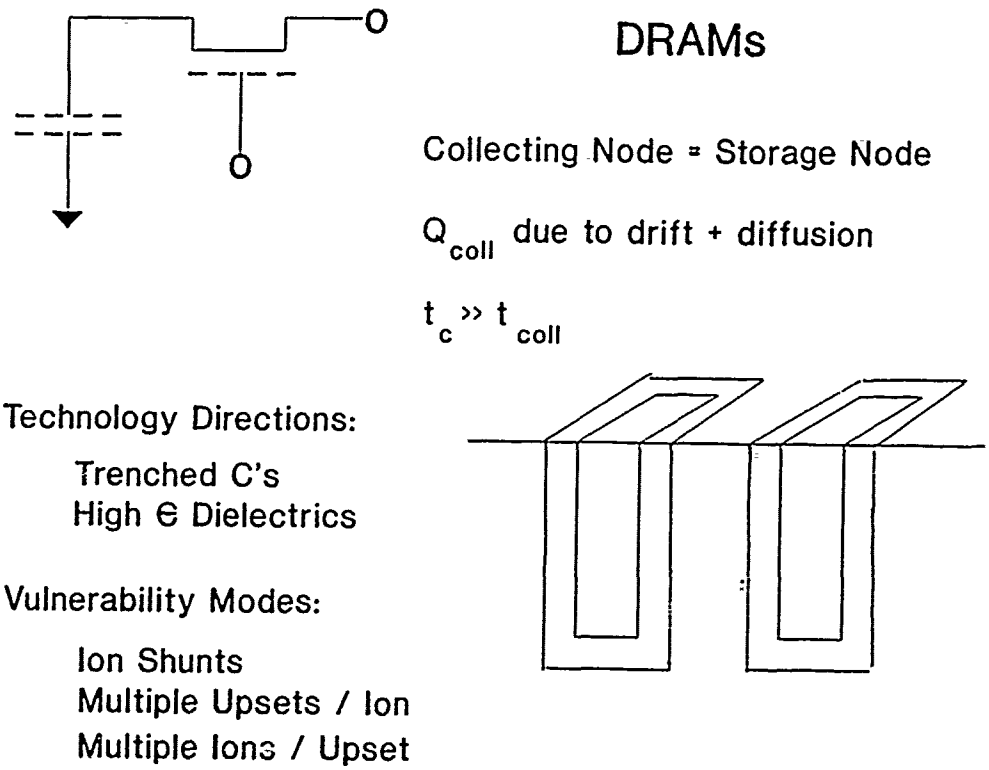


Figure 32. Trenched-capacitor DRAM characteristics.

Anticipated directions for the evolution of TCDRAM technology include the use of high dielectric-constant and/or ferroelectric materials for the charge-storage capacitors, and the incorporation of isolation technologies to place each cell or some small group of cell in dielectrically isolated regions. Both of these directions would increase the amount of charge stored per unit supply voltage and feature size, making them "harder" to single-event upset. The possibility for dielectrically isolated TCDRAM technology holds the promise of removing the potential for upset due to ion shunt effects and the potential for a single ion creating multiple upsets.

4.3.2 Resistive-Load SRAMs.

Resistive-load SRAMs (RRAMs) have become the highest density of all SRAM technologies with the advent of multilayer interconnect capability, which allows the resistive loads to be fabricated in regions overlying the active RAM transistors. RRAMs today use extremely high resistance loads (with gigaohms resistance) fabricated in undoped polysilicon. These are not true "loads" in that they provide very little current to the information nodes. Their purpose is to resupply the

small amount of current that leaks off of the drains of the cross-coupled transistors in the RAM. In this way, RRAMs are much like cross-coupled DRAMs. Figure 33 summarizes the characteristics of RRAMs relevant to their single-event vulnerability, and shows two schematics of an RRAM cell -- one shows the resistive loads, while the second omits them. This second form has been used in the literature to emphasize the fact that the resistive loads are not active elements in the circuit function as a RAM, they merely compensate for non-idealities in junction leakage. Because RRAMs effectively have no load resupply, they must be written from both sides simultaneously.

RR' 1s

Collecting Junction = drain/substrate
Storage node = drain + gate
Q_{coll} due to drift + diffusion
$t_c \gg t_{coll}$

Technology Directions:
Loads in overlayer
Trenched Drains

Vulnerability Modes:
Multiple Ions / Upset

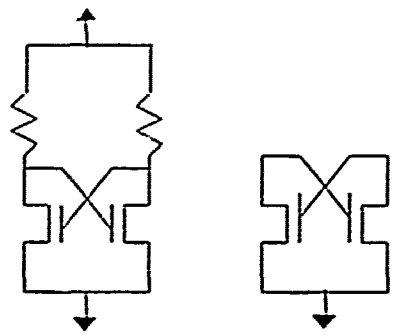


Figure 33. Resistive-load SRAM characteristics.

While RRAMs are much like cross-coupled DRAMs, this coupling does allow a spatial distribution of information storage in the cell and makes them essentially invulnerably to multiple upsets from a single ion event. They do, however, share with DRAMs a long integration time, and are vulnerable charge collected by both drift and diffusion, as well as to a single upset due to the cumulative effects of multiple sub-critical hits.

RRAM designs are compatible with trenched technologies and with isolation technologies. These approaches can be anticipated as future directions for RRAM evolution.

4.3.3 CMOS SRAMs.

CMOS SRAMs have long been a stalwart of the radiation-hardened electronics community, due to their low power consumption, packing density and technology maturity. They have served as a platform for some of the most effective hardening approaches discovered to date, primarily involving coupling elements to delay the arrival of the single-event perturbation at information storage nodes until the active loads could resupply the original charge state of the hit node [71, 106-108]. The features of CMOS SRAMs pertinent to predictions of single-event vulnerability are summarized in Figure 34. They have the distributed information storage characteristic of all SRAMs, and, due to their switching speed are the first of the technologies considered here to be vulnerable only to prompt charge collection from single events (i.e., they are not susceptible to upset by the slower diffusion-collected charge).

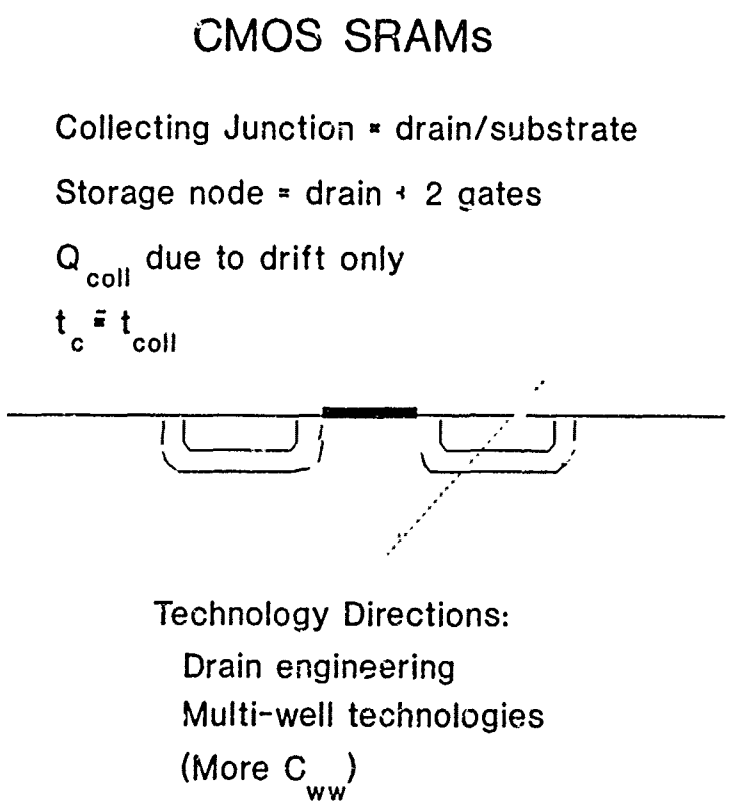


Figure 34. CMOS SRAM characteristics.

The "constant field" scaling rules, when written, applied to CMOS (and the MOS transistors in BiCMOS), but present technologies have evolved along a path somewhat skewed from those rules. Technology trends are toward smaller channel lengths, increased device packing density, higher

doping levels, thinner gates -- all predicted by constant field scaling, but the precise relationships between these characteristics do not follow the simple rules of the constant-field model. Nevertheless, constant-field scaling provides a guide to CMOS evolution. In cases where its rules cannot be met, innovative solutions to maintain "true" CMOS device characteristics have been found. Examples of these innovations include drain engineering and multi-well technologies. For both of these types of innovations, many examples exist. The primary example of drain engineering is the use of "lightly doped drains" (LDD) structures, in which a double implant forms the drain and source nodes of the devices. The majority of the drain region is degenerately doped, as in past generations of CMOS. Thinner, more lightly doped regions extend from the major drain and source regions toward the gate. These regions reduce the field supported by the depletion region near the drain edge in ON transistors; reducing this field diminishes the injection of carriers from the channel into the gate oxide and improves reliability without requiring lower voltage supply levels for the IC. [The ability of CMOS designers to maintain a single voltage supply level for years at a time, at 10 V then at 5 V perhaps next at 3.3 V, has allowed the technology to remain compatible with others, even as its feature lengths have shrunk and its capabilities increased. Such standardization would not have been possible with constant-field scaling, which demands changes in supply voltage with each reduction in feature size.] Multi-well technology approaches include twin-well and quadruple-well approaches; these are extensions of well profile tailoring, which has evolved over many years to maximize the performance of both transistor types.

Another trend of CMOS technologies is to have increasingly larger parasitic capacitances, notably capacitances between electrical interconnects (C_{ww}). The effect of these capacitances is to decrease the portion of total chip capacitance under active control, and thereby to reduce noise margin. Further innovation is require to maintain suitable noise margin as device sizes shrink.

4.3.4 CMOS/SOI-SOS SRAMs.

An evolution of CMOS technology designed to increase speed and/or radiation hardness is CMOS/SOI, CMOS in silicon-on-insulator. While this term is generic, and strictly includes CMOS/SOS, CMOS in silicon-on-sapphire, CMOS/SOI is often used to refer specifically to a silicon-on-silicon dioxide, or "SIMOX" technology. These are examples of "insulating technologies" in which active layers are fabricated overlying insulating layers. Such structures have several advantages, including smaller capacitances, both parasitic and intentional, than their bulk-technology counterparts, thinner collecting volumes and the potential for extremely high packing density, because wells are not necessary.

With the advantages due to thin active overlayers on an insulating substrate layer come some characteristics which alter the characteristics of CMOS/SOI device characteristics. Since the "back" of the channel region abuts an insulating layer, methods used in CMOS bulk and epi technologies to electrically control the "back channel" of the MOS transistors cannot be used.

Section 3 of this report is devoted to the analysis of the vulnerability of CMOS/SOI SRAMs to single-events. The characteristics of CMOS/SOI technologies pertinent to the scaling of their single-event vulnerability are summarized in Figure 35.

CMOS/SOI-SOS SRAMs

Collecting Junction = drain/body

Storage node = drain + 2 gates

Q_{coll} due to drift; amplified by B

$t_c = t_{coll}$; $Q_{coll} < Q_{crit}$

Technology Directions:

Thin Overlayers

Drain engineering

Fully depleted bodies

(Low parasitic capacitances)

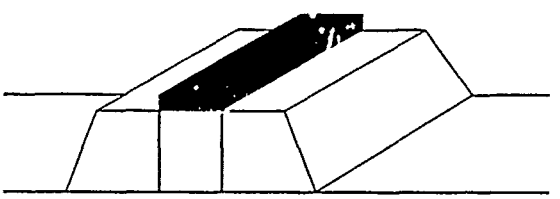


Figure 35. CMOS/SOI SRAM characteristics.

CMOS/SOI technologies have the advantages of other CMOS relevant to information storage (distributed) and collected charge vulnerability (prompt). They also share with other CMOS technologies their trend toward drain engineering as they scale. Additional scaling directions include the thinning of active overlayers to allow fully depleted body regions during ON operation.

As discussed in detail in section 3 of this report, CMOS/SOI technologies differ in at least one important respect from their bulk counterparts in their response to single events: the parasitic bipolar inherent in the CMOS/SOI transistor *amplifies* the charge collected from an impinging ion. For this reason, CMOS/SOI SRAMs can be upset even when the collected charge from the single event (Q_{coll}) that initiates upset is less than the critical charge (Q_{crit}) of the RAM cell (because Q_{coll} is augmented by the bipolar action; the amplification factor is equal to the current

gain of the parasitic bipolar, β, which can be large, especially for transistors with small channel(base) lengths(widths)).

4.4 DEFINING SENSITIVITY SCALING.

4.4.1 Constant-Field Scaling Rules and Their Violations.

Figure 36 summarizes the constant field scaling rules [87], and their consequences on the scaling of critical charge. It shows how various device and circuit parameters, including the channel length, l, the supply voltage, V, the gate oxide thickness, t_{ox}, the doping density, N_D, the capacitance, C, the resistance, R, the total power, P, the current density, J, and the circuit density, D, change as the channel length is decreased by a factor k.

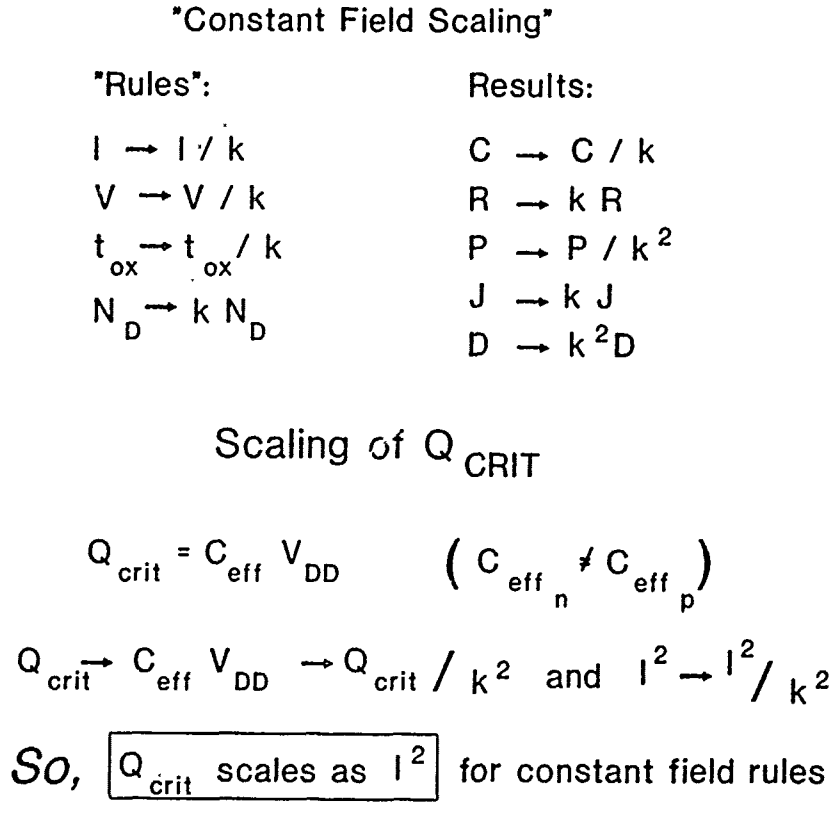


Figure 36. Constant field scaling of Q_{crit}.

Early work on single-event vulnerability [71] showed that, for a given CMOS SRAM, vulnerable to two types of hits -- those to OFF n- and OFF p-channel drains -- the simulated critical charge for upset scaled linearly with supply voltage, VDD over the entire range of voltages for which

the circuit was functional. As a linear relationship between charge and voltage implies a constant capacitance, an effective capacitance, C_{eff}, was defined for each vulnerability mode; since the slope of Q_{crit} vs. VDD plots are different for p-hits and n-hits, $C_{effn} \neq C_{effp}$. It may be at least interesting, if not conclusive, that the relationship $Q_{crit} = C_{eff}$ VDD provides a basis for predicting the scaling of critical charge for single-event upset with feature size (at least under constant-field scaling rules) as the scaling of capacitance and supply voltage are given by those rules. The resulting scaling prediction is that Q_{crit} scales as the square of the channel length or feature size, l^2. This result confirms the well known "Petersen Law" depicted in Figure 37.

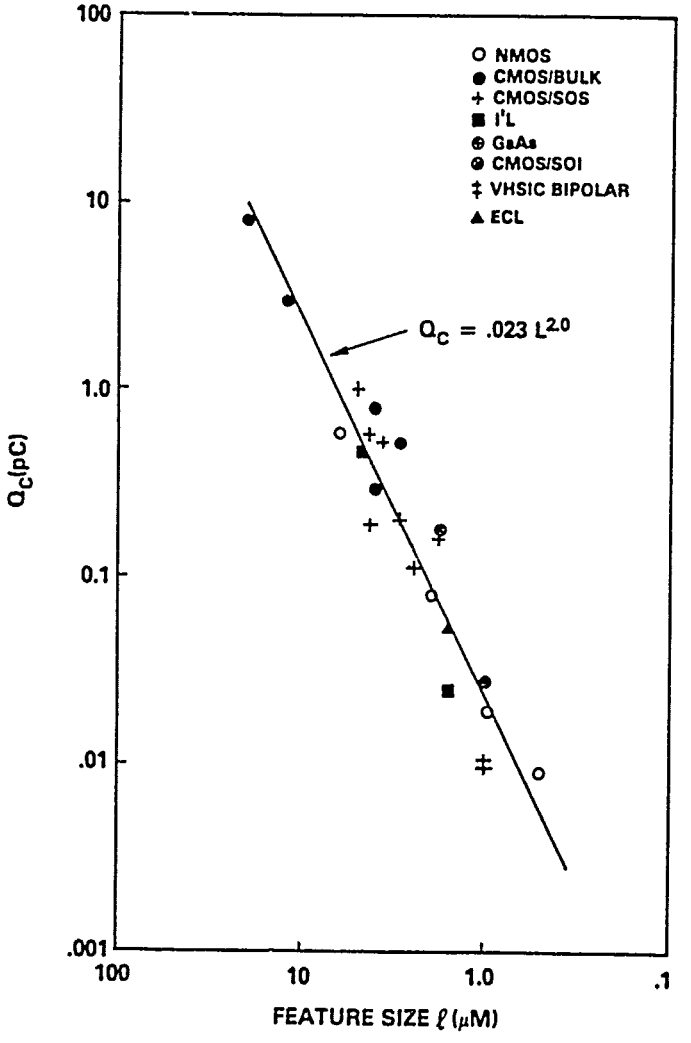


Figure 37. Q_{crit} vs. feature size.

For the "technologies of the future" identified here, constant-field scaling rules do not apply, at least in full. The proportionality of critical charge and the square of feature size, if it truly require constant-field scaling, then also requires that $Q_{crit} = Q_{coll}$ (i.e., does not allow for parasitic amplification of single-event collected charge), and also requires that the collecting volume and

storage or effective capacitance are directly related to the feature size. Figure 38 summarizes these requirements and lists those requirements that are or can be anticipated to be violated in the four technologies covered in this section.

$$Q_c \propto l^2$$

requires:
1. $Q_{crit} = Q_{coll}$
2. collecting volume related to l
3. storage C related to l
4. constant field scaling

Anticipated Violations of Requirements

DRAMs	2, 3, 4
RRAMs	2 (4)
CMOS SRAMs	(4)
CMOS/ISO SRAMs	1, 3 (4)

Figure 38. Requirements for Petersen scaling.

Trenched DRAMs blatantly violate constant-field scaling rules, as their storage and collecting volumes and hence their storage capacitances are predominantly determined by the depth of their trenches, rather than by their feature sizes; RRAMs violate because they collect diffusion charge; CMOS SRAMS, as stated above, do not precisely follow constant-field scaling; CMOS/SOI RAMs share this CMOS attribute and have the additional violations of a storage capacitance not related to feature size (rather to overlayer thickness and device *width*) and a Q_{crit} unequal to Q_{coll}, as discussed above.

4.4.2 Sensitivity of Future Technologies to SEU.

As we are left with technologies predicted to expand in their future applications which do not follow constant field scaling rules, and are left without scaling rules for those technologies, the best that can be offered here is a suggested measure for the sensitivity of technologies to single-

event upset. This is, obviously, a measure of the relative change in *threshold* for single-event upset for future technologies; it is not analogous to the "figure of merit" [90] which predicts upsets per bit-day. This sensitivity measure, defined as 1/S, depends on the scaling of Q_{crit} to Q_{coll}.

For TCDRAMs and RRAMs,

$$S = \frac{1}{T} \int_{t_o}^{T} \left(\frac{1}{Q_{coll}} \right) \left(\frac{d\, Q_{crit}}{dt} \right) dt$$

where t_o is the time when the maximum intended charge is stored (Q_{crit} is maximum, i.e. immediately after a refresh or a write), and T is the refresh period for TCDRAMs and the period for charge restoration through the high resistance loads for RRAMs.

This relationship demonstrates the effect of diminution of Q_{crit} over time due to leakage in these technologies on device vulnerability to single events.

For CMOS bulk and epi technologies, the relationship is quite simple,

$$S = \frac{Q_{crit}}{Q_{coll}}$$

It must be noted that in general p- and n-channel devices within an SRAM (or any other type of digital logic) will have different values of both Q_{crit} and Q_{coll}.

For CMOS/SOI technologies,

$$S = \frac{Q_{crit}}{(\beta + 1)\, Q_{coll}}$$

where β is the current gain of the parasitic bipolar device; again all variables in this expression are different for different device channel types.

To quantify these sensitivity measures, one would have to evaluate the effects of relevant technology characteristics that do not scale. Table 8 gives a list of the "top ten things that don't scale", and indicates the effects of these non-scaling parameters on critical and collected charge. Again, this is a quantitative representation, but it shows that non-scaling parameters *all* conspire to increase the sensitivity of future technologies to single-event upset.

Table 8. Top ten things that don't scale.

Q_{crit}	Q_{coll}	
↓		1. Junction Leakage
↓		2. Subthreshold Current
↓		3. Gate Capacitance Control
↓		4. Gate-Drain Capacitance
↓		5. Parasitic Wire-Wire Capacitance
↓		6. Parasitic Wire-Underlayer Capacitance
	↑	7. Lateral bipolar betas
↓		8. Contact Resistances
?	?	9. P/N Saturation Currents & Channel Mobilities
↓		10. Body Effects

4.4.3 Scaling of Error Rate.

Figure 39 shows the effect of constant field scaling on the figure of merit for single-event error rate [90]: when constant field scaling rules are applicable, error rate remains constant. This conclusion was also reached in previous studies on scaling [88, 89].

The problem in interpreting these results for the scaling of error rate come when one considers the meaning of Q_c. As the alternative form for the figure of merit [90] uses the equivalency $Q_c/c = LET_c$ (where the variable c is the smallest of the sensitive volume dimensions, intended to be the thickness of the sensitive junction). This equivalency indicates that $Q_c = Q_{coll}$. Thus, this figure of merit for error rate is based on several assumptions:

i. the sensitive volume and the collecting volume are proportional

by Constant Field Scaling Rules:

$$E = R\,a\,b\left(\frac{c}{Q_c}\right)^2 \longrightarrow \frac{R\,a\,b}{k\,k}\left(\frac{c\;k^2}{k\;Q_c}\right)^2 \longrightarrow \text{constant}$$

BUT: What is Q_c?

$$Q_c = Q_{coll}$$

Error Rate is Constant with Scaling Provided:

$Q_{crit} = Q_{coll}$ (CMOS only)

"Constant Field" rules are valid (CMOS only)

Sensitive & Collection volumes simply related (CMOS, RMOS)

Critical Charge is constant in time (CMOS, CMOS/ISO)

Figure 39. Scaling of error rate.

ii. the amount of charge collected from a single event is related to the smallest dimension of the sensitive volume

iii. the critical charge for a given device is constant in time.

iv. the charge required to upset a device (Q_{crit}) is equal to the charge collected from a single event.

As emphasized in the above discussion and summarized in Figure 39, these conditions **do not hold** for future technologies. This means that the figure of merit for error rate **is not accurate** either for the prediction of single-event vulnerability in these technologies, or for a prediction of how this vulnerability will scale.

As an author of the original figure of merit paper, I feel that these conclusions should be considered with considerable weight. The figure of merit was never intended to be a precise measure. Even in the original paper, it was pointed out that it accurately depicted the *trends* in upset rate for the (older) devices it analyzed. Nevertheless, it has been a convenient tool for the

evaluation of single-event vulnerability for ICs. **It has been applied beyond its range of accuracy.** As can be deduced from the foregoing (especially the sensitivity relationships and Table 8), *actual* scaling trends tend to make the figure of merit **overly conservative.** Some system reliability estimates, based on this figure of merit, especially those for systems using advanced parts of the types highlighted here may be erroneous.

In order to assure the hardness of future technologies to single events, the issue of a *valid* measure for upset sensitivity and for error rates must be addressed anew.

4.5 CONSIDERING PROBABLE FUTURE VULNERABILITIES TO SEU.

To reiterate, the lack of quantitative information on actual scaling rules for the technology types covered in this report precludes quantitative predictions of the scaling of their vulnerability to single-event upset. Still, some qualitative predictions (divinations?) can be made, based on the point raised above.

4.5.1 Directions of Future DRAM Vulnerabilities.

The advent of trenched-capacitor DRAM, TCDRAM, technology brings with it greatly enhanced charge storage per bit and per unit feature size. Therefore TCDRAMs can be expected to be significantly less sensitive to single-event upset than their planar-technology counterparts and also to demonstrate lower error rates in a given environment.

4.5.1.1 The Good News. If (as) the technology moves toward high dielectric constant or ferroelectric materials for storage capacitors, this enhancement will be even more pronounced. And *if*, in addition, TCDRAMs can be fabricated in an isolation technology, there exists the possibility that a TCDRAM can be designed to store more charge than it can collect from a single ion interaction, i.e., the possibility for **single-event "immune" TCDRAMs.** Because of the extreme vulnerability of past generations of DRAM technologies to single events, they have long been ignored as a potential approach to hardened RAMs. This should not continue, if high dielectric capacitors and isolation technologies can be integrated with TCDRAM technology. Should this happen, TCDRAMs may provide the **densest hardened RAM technology.**

4.5.1.2 The Bad News. Of course, as in other isolation technologies, DRAMs have two additional "problems" that have limited their use, especially in high reliability, autonomous systems. junction leakage (already a primary concern for information retention in DRAMs) and power dissipation (high in DRAMs in general, because of the need for refreshes to restore charge lost via leakage). These "problems" are well known to be exacerbated in total-dose environments.

4.5.1.3 The Bottom Line. While the difficulties involved in incorporating high dielectric or ferroelectric materials into any technology should not be trivialized, and the difficulties in integrating TCDRAM fabrication into an isolation technology such as SOI and controlling leakage in cells effectively surrounded by insulating interfaces may be at least as great, future TCDRAM technologies have considerable promise for extremely high density, fast logic not vulnerable to single events. In the case of a DRAM technology, it is especially important to make those who guide (cajole, force) technology directions aware of this promise, as past DRAMs have not been suitable candidates for radiation-hardened systems applications, and the community at large has for many years not considered developing or even investigating DRAMs for these applications.

4.5.2 Directions of Future RRAM Vulnerabilities.

RRAMs, though they have the potential for integration with high dielectric capacitors and isolation technologies described in the previous subsection, are less likely to move in those directions than are TCDRAMs. RRAMs have generally been used for commercial applications. In radiation environments, they are relatively more sensitive to single-event upset, multiple-event upset and total-dose upset than their CMOS counterparts. As compared to planar DRAM technologies, they have been less vulnerable to single events, although this advantage may well not hold as TCDRAM technologies advance.

4.5.2.1 The Bad News. It appears that there is very little good news, so long as RRAM technology remains in the commercial sector. RRAMs will evolve to higher densities, but unless they incorporate trenched drains and/or insulating substrates, they cannot be expected to show improved resistance to single-event upset; they would evolve to be more sensitive to single-event upset and show higher error rates. *IF* they incorporate these changes, becoming effectively cross-coupled TCDRAMs, they would show the same considerable advantages for radiation-hardened applications noted above for TCDRAMs. However, such TCDRAMs may be hard enough in and of themselves, so that the added complexity of analogous RRAMs may be unwarranted.

4.5.2.2 The Bottom Line. RRAMs have the least potential for future single-event hardened digital logic of the technologies considered here.

4.5.3 Directions of Future CMOS SRAM Vulnerabilities.

CMOS SRAMs provide the most mature of the technologies considered here for hardened ICs. Hardening techniques, not only for single-event upset, but also for total dose failure and dose-rate upset, have benefitted from a large body of successful processing, circuit design and chip layout advances, and analytical tools and hardness-assurance testing methods supporting analyses of the radiation vulnerability of CMOS ICs are also mature. The radiation-hardened electronics community can certainly be expected to continue its reliance on CMOS for years to come.

4.5.3.1 The News. Numerous innovative approaches to hardening CMOS to single events have been implemented, as detailed above. For clarity, however, let use first consider "raw" CMOS, without added elements decoupling SRAM nodes: as such CMOS scales to ever smaller feature sizes, it will become increasingly vulnerable to single event upset, though this increasing sensitivity can be moderated by multi-well technologies and by creative substrate doping profile approaches. It is interesting, however, that even in this "unhardened" CMOS error rates should not signific ntly increase, even though sensitivity to upset increases. This relatively constant error rate for scaled devices (elucidated in Figure 39 above) derives from the assumptions of constant-field scaling rules and the applicability of the presently accepted figure of merit for single-event error rates; it is due to the fact that the tendency for error rate to increase with decreasing feature size is precisely compensated by the decrease in error rate due to smaller total sensitive areas in scaled ICs. As stated above, CMOS evolution has not strictly followed the constant-field rules (however the directions of scaling of CMOS device and circuit parameters have complied with constant-field scaling trends), and there is also reason to doubt the applicability of the figure of merit for scaled devices. For this reason, the prediction of relatively constant error rates for unhardened, scaled CMOS ICs may be overly optimistic.

CMOS single-event hardening techniques have successfully lowered error rates to the levels demanded by ultra-hard systems, but not without a price. For present technologies, resistive cross-coupling approaches have required increases in RAM cell size and dictated decreases in cell speeds, approaches adding drain-resistance reduce this speed penalty, but also reduce the noise margin of cells and may therefore be unacceptable for aggressively scaled devices. Other approaches, detailed in restricted literature, can moderate the penalties associated with these resistive hardening techniques.

CMOS technologies have already incorporated insulating substrates (see the next subsection) and may incorporate high dielectric constant or ferroelectric materials to significantly increase their charge-storage capacitances. This latter direction can significantly reduce single-event vulnerability *and* error rates.

4.5.3.2 The Bottom Line. The set of techniques and approaches presently available to decrease the single-event vulnerability of CMOS SRAMs is the largest for any technology. The technology is mature, has multiple vendor sources, and many of its designers are knowledgeable regarding single-event effects. Commercial, unhardened CMOS is probably the "naturally" hardest of commercial technologies. For these reasons, the radiation-hardened electronics community is certain to continue to rely on CMOS ICs and to encourage their continued hardening development.

4.5.4 Directions of Future CMOS/SOI SRAM Vulnerabilities.

CMOS/SOI technology has made enormous progress recently. The quality of silicon overlayers, the pacification of insulating substrate interfaces and device side walls and the enhancement of

device yields have proceeded extremely rapidly, so that a technology that was merely a "good idea" only a few years ago is now sufficiently mature and reliable to enjoy widespread applications, not only in the radiation-hardened IC community, but also in the commercial sector. CMOS/SOI technology is an example of an approach in which commercial advantages (speed, packing density) "naturally" accompany advantages in circuit hardening to single events (reduced collection volumes and sensitive areas). For these reasons, CMOS/SOI has received considerable support from both government and industry and accelerated its development at a pace more rapid than any other technology over the past few years.

4.5.4.1 The Good News. CMOS/SOI enjoys the advantages noted in the previous subsection for all CMOS technologies. In addition, the insulating layer under its thin active overlayers truncates charge collection from single events, greatly reducing the charge collected onto sensitive nodes relative to that collected by bulk or epi CMOS designs of the same feature sizes (and similarly reducing charge collected in dose-rate environments). These characteristics make even un-single-event-hardened CMOS/SOI SRAMs inherently harder to single-event upset than their bulk counterparts. In addition, CMOS/SOI SRAMs with fully bottomed junctions have considerably less capacitance per unit area than their bulk/epi counterparts, making them faster, and CMOS/SOI designs do not require junction isolation between p- and n-channel transistors (do not require wells), making these designs denser than their bulk/epi counterparts.

4.5.4.2 The Bad News The parasitic transistor inherent in CMOS/SOI transistors acts to amplify the charge collected from single events and can, thereby, allow SRAM cells to upset even when they collect less than their critical charge. This is not a characteristic of present CMOS bulk or epi technologies. As device dimensions shrink in future generations of CMOS/SOI SRAMs, this effect will increase, even for fully depleted transistors. Body ties cannot remove this effect, as detailed in section 3 of this report. It is also important to recognize that the assumptions of constant-field scaling are not valid for CMOS/SOI technologies, and that the presently accepted figure of merit for error rates is not valid for CMOS/SOI technologies (see Table 11 above).

4.5.4.3 The Bottom Line. The success of future generations of CMOS/SOI technologies in applications requiring radiation-hardened ICs strongly depends on "solving" the problems due to parasitic bipolar action. Several approaches used in the past in other technologies for reducing parasitic βs may be applicable to CMOS/SOI; the problem should not be a "show stopper" but must be addressed to garner the promise of CMOS/SOI. If the current gains of parasitic bipolars can be controlled, and if progress on controlling charge build-up in insulating layers and at insulator interfaces continues, thin overlayer CMOS/SOI will be the technology of choice for systems requiring single-event hardness. Its potential in this arena can be reached with the fewest technology changes of any of the technologies addressed here.

4.6 CONCLUSIONS.

The issue of how single-event upset will scale in future technologies must first incorporate predictions on what those technologies will be. Here, four promising technologies have been identified and discussed. trenched-capacitor DRAMs (TCDRAMs), high resistance load SRAMs (RRAMs), CMOS bulk or epi SRAMs, and CMOS/SOI SRAMs. Given the absence of information on how these devices are being scaled at present and will be scaled in the future, it is not possible to make quantitative predictions of their future vulnerabilities to single events.

Despite the unavailability of scaling information, several qualitative predictions can be made, based on assumptions about what future innovations may be incorporated into present technologies. These predictions suggest that RRAMs have little promise for future radiation-hardened IC applications, and that CMOS bulk and epi technologies will continue, at least for the next several years to be useful.

The promise for TCDRAMs is considerable, yet the potential of this technology for radiation-hardened applications seems to have been ignored to date. This promise will be fully realized only if either high dielectric constant or ferroelectric capacitances can be used, or if TCDRAMs can be fabricated in isolating substrate materials, or both. These technology advancements will require considerable development, but if they are realized, TCDRAMs offer *extremely* high density ICs with the potential for high radiation hardness.

CMOS/SOI SRAMs presently offer the greatest promise for near-term, ultra-hard ICs. This promise hinges on thinning overlayers (an effort already garnering considerable attention) and on reducing the parasitic bipolar current gain. The technology advances required to reap the potential benefits of hardened CMOS/SOI are considerably less complex than those required to bring TCDRAMs to the same level. Still, TCDRAMs should be explored, and efforts to advance this technology should be encouraged, for they could well prove to supersede CMOS/SOI SRAMs in both overall performance and in radiation hardness.

Finally, a very important point encountered during the course of this research is that the presently accepted figure of merit for predicting single-event error rates of digital ICs is not applicable to many present and planned future technologies. If we are not to get "caught" fielding vulnerable systems based on incorrect analyses of their predicted error rates, we must revisit the issue of a figure of merit and derive a new measure accurate for today's and tomorrow's technologies.

SECTION 5

GaAs SINGLE EVENT EFFECTS

5.1 INTRODUCTION.

Errors produced in solid state circuits due to high energy single particles have become of increasing importance in recent years. Semiconductor memories are the most susceptible to ionizing particles because of their small feature size, and low nodal capacitance. Errors in silicon RAMs have been attributed to cosmic rays [109] and to alpha particles from the radioactive decay of trace impurities in ceramic packages [110]. Memory design for space applications requires thorough insight into the circuit upset mechanisms. Single event upset (SEU) mechanisms in silicon MOS technologies differ in several important ways from effects seen in GaAs MESFET and JFET memories. GaAs FET memories are affected by two upset mechanisms, quantified by gate-to-drain and source-to-drain critical charges. Upset levels for GaAs memories are dependent on nodal capacitances, the time profile of charge collection from single events, intrinsic circuit time constants, and logic voltage swings. These circuit upset parameters are analyzed using accurate circuit simulation models in this work to predict circuit upset thresholds. SPICE-based simulations have been used to investigate GaAs E/D, C-EJFET, and D-MESFET/resistor memories.

Gallium arsenide has been used as a substrate material for discrete devices for many years. However, in recent years lithography advances, reduced costs, and improved substrate material have made GaAs LSI circuits commercially feasible. Static memories in GaAs have been realizable since 1981 [111]. GaAs FET technologies incorporating SRAMs have been based on (1) enhancement/depletion MESFETs (E/D MESFET) [112] , (2) complementary enhancement junction FETs (C-EJFET) [113], (3) enhancement/depletion MODFETs (E/D MODFET) [114], (4) D-MESFETs/resistor [115], and (5) D-MESFETs/D-load [116]. SRAMs in these technologies have been manufactured in size from 256 bit to 16Kbits, but yields have been low.

The limited supply of GaAs SRAMs, and the few available SEU test sites have made GaAs SEU data sparse. Presently only three designs in two technologies are known to have been tested for soft errors: the C-EJFET technology [117], a rad-hard C-EJFET [118], and the D-MESFET/resistor technology. Experimental results show unhardened GaAs SRAMs are equally or more susceptible to single event upset than silicon memories. A hardened design of a C-EJFET memory has shown that resistive decoupling can be used to reduce soft error rates (SER) [118].

The limited quantity of GaAs experimental data has made circuit simulation an important tool for studying SEU response in GaAs. Circuit simulation results have correlated very well with experimental SEU data [119] and continued GaAs circuit and device analysis is needed to provide a complete understanding of GaAs IC reliability in space environments.

5.2 BASIC SEU MECHANISMS.

Protons, heavy ions and alpha particles comprise particles capable of producing soft errors. High energy particles produce a high density track of electron-hole pairs in a semiconductor. These carriers are transported by drift and diffusion to the junctions resulting in photocurrents. The collected current pulse consists of a fast component and a slower diffusion component. The fast "prompt" or "drift" component consists of charge from the junction depletion region and, (if the created carrier density exceeds the background doping) from an added distance within the device known as the funnel length. GaAs devices on semi-insulating substrates have a funneling contribution which is small (less than 10%) compared to silicon, because of the long dielectric relaxation time and short minority carrier lifetime of semi-insulating GaAs [120].

The diffusion or delayed component includes charge carriers collected by diffusion to the depletion regions after the depletion region has recovered. The minority carrier lifetime in GaAs (τ = 10^{-10} to 10^{-9} seconds) is approximately 10^5 times less than in silicon. This is primarily because GaAs is a direct gap material. Therefore the diffusion component of collected charge is smaller in GaAs than in silicon devices.

The time profile of the photocurrent pulse is not well characterized but is frequently approximated by a double exponential rising and falling pulse. Photocurrent measurements for GaAs Schottky diodes on semi-insulating substrates [120,121] have bounded the pulse shape parameters: rise time is less than 120 ps (equipment limited), and fall time less than 300 ps. The time integral of the photocurrent or the magnitude of total charge needed to change the state of a memory latch, is referred as the critical charge. Simulations to be discussed later have shown that critical charge of GaAs SRAMs is dependent to some extent on the fall time of the pulse [119].

A major difference between GaAs MESFETs and Si MOSFETs is the location of nodes vulnerable to current pulses resulting from a high energy particle. The MOSFET, being an insulated gate structure, is destabilized by a current pulse between the drain and substrate or source, corresponding to a particle hit on the drain. MESFETs by contrast do not have insulated gates. Thus they can collect charge from particle hits on their gates. Such events produce a current pulse between the gate and drain. Events between the gate and source are not as important because the charge collection between gate and source is small compared to the collection between gate and drain of the vulnerable transistors (i.e. there is a smaller E-field and depletion region in the gate-to-source region as compared to the gate-to-drain region of an OFF device). This simulation prediction has been confirmed by Flesner [122] by demonstrating that single-event upsets can be induced by an E-beam incident between gate-and-drain. Upsets were not observed by an E-beam incident between gate-and-source. MESFETs are also destabilized by the drain-to-source currents which can similarity upset MOSFETs. Previous modeling analyses have used an exponentially decaying current source to represent source-to-drain charge collection in MESFETs. It has recently been recognized that such a current source can force the drain node of an OFF n-device to become negative, a physically unrealizable condition.

Therefore the model of a single-event perturbation between the source and drain has been changed in the work reported here. The source-to-drain collection is modeled using an exponentially decaying resistance between source and drain (corresponding to the change in channel conductance). Circuit-level models for charge collection from single events penetrating the GaAs MESFET or JFET depletion regions use a photocurrent source between gate-and-drain, and an exponential time-dependent resistance between source-and-drain. Figure 40 shows a cross-section of a JFET and the location of these charge collection modeling elements. The gate-hit vulnerability distinguishes GaAs MESFET and silicon MOSFET ICs; hardening approaches using only gate resistors (to be discussed later) are not effective in hardening to perturbations at the gate.

Critical charge is only one of the key parameters needed to describe SEU vulnerability of a circuit. An approximate expression developed by Petersen, et al., [123] which describes the SEU error rate in errors/bit-day is

$$SER = K \cdot 10^{-10} \cdot ab \left(\frac{c}{Q_{crit}} \right)^2, \qquad (1)$$

where K is a multiplicative constant, ab is the sensitive device area, c is the charge collection depth and Q_{crit} is the critical charge. The multiplicative constant for GaAs is equal to 3.35 and is derived from experimental measurements [124]. Comparison between different GaAs technologies using Equation (1) may be useful and justified but comparisons between silicon and

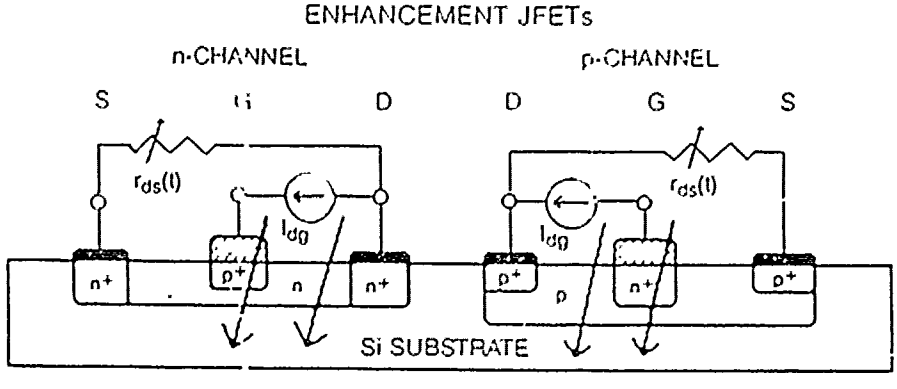


Figure 40. JFET Photocurrent locations.

GaAs devices must consider that the proportionally factor is material dependent. (In silicon the proportionally factor is equal to 5.0). Sensitive volumes have been estimated for gate-to-drain and source-to-drain collections from layout information [125].

5.3 MAJOR FACTORS DETERMINING GaAs SRAM SEU VULNERABILITY.

Information is typically stored in a RAM cell by the state of two cross-coupled inverters. Source-to-drain and gate-to-drain photocurrents produce soft errors by reversing the states of the transistor pairs. To cause upset, the particle photocurrents must produce enough charge to change the voltage state of critical nodes in the RAM cell. Figure 41 shows possible circuit locations of photocurrent elements in a memory cell schematic. The two elements act in fundamentally different ways to cause RAM cell upset. Source-to-drain photocurrents, modeled by the time-dependent resistor, drop the drain voltage of OFF devices and sink charge from gates of ON devices, while the gate-to-drain photocurrents supply charge to gates of OFF devices, turning these devices ON.

The memory cell error is not permanently latched until both driver transistors have changed their gate bias conditions. A source-to-drain photocurrent first switches the gate bias of the unhit transistors in the opposite inverter (F2 and F4 in Figure 41), and discharges the capacitance of the hit OFF node. These changes shift the bias state of the hit transistor, resulting in logic upset. The source-to-drain photocurrent perturbs gate voltage via the latch's feedback mechanism. The gate-to-drain photocurrents directly charge the hit device's gate capacitance, holding its channel open, and switch the gate bias of the unhit inverter. The gate-to-drain collection directly affects both the perturbed transistor's gate and channel.

Critical charge in these situations can be described by Equations (2) and (3), which relate event-induced photocurrent, nodal capacitance and circuit voltage levels to critical charge [125].

$$Q_{crit} = Q_{co} + Q_s, \qquad (2)$$

and

$$\int_0^{t_1} I_{col}\, dt = \frac{1}{t_1}\int_0^{t_1} C_{node}\, dt \cdot V_{co} + k \cdot \int_0^{t_1} I_s\, dt, \qquad (3)$$

where t_1 is the length of the current pulse. Critical charge can thus be described by two components: (i) the charge required for cell upset in the static case (Q_{co}), and (ii) the charge being removed from the hit node during the photocurrent pulse (Q_s).

In Equation (3) I_{col} is the amplitude of the current source modeling the event, C_{node} is the nodal capacitance, and V_{co} is the voltage needed to change the logic state of the cell. An empirical constant describing the ratio of nodal current to total cell current is given by k. Finally I_s is the total current drawn from any voltage supplies connected to the memory cell.

Differences between GaAs technologies can be expressed in terms of C_{node}, V_{co}, I_s, and k in Equation (3). Capacitance is not only a critical factor in determining the single event response, but is also a major factor in determining circuit speeds. Layout parasitic capacitance and device capacitance contribute to the term C_{node}. Layout capacitance is dependent on the metal

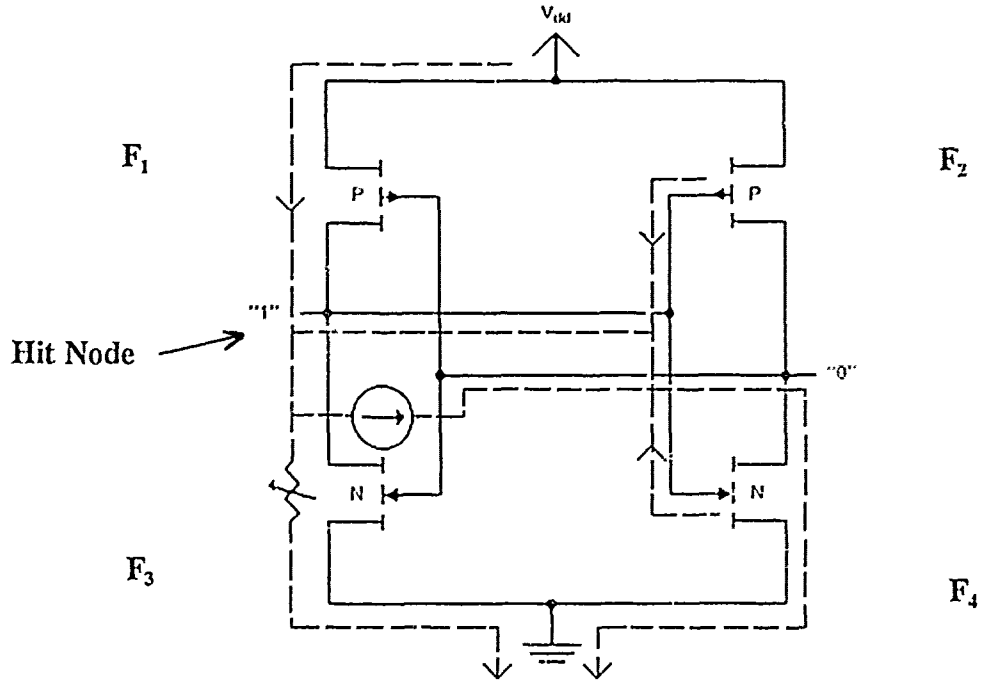


Figure 41. Photocurrent paths in a C-EJFET RAM cell.

interconnects and passivation layer thickness. Of the GaAs technologies examined, layout capacitances were comparable for comparable feature sizes and scales of integration. Device capacitances are determined by device area, doping, and contact type and are controlled by channel doping, and channel depth. The two enhancement devices which have been studied use similar doping levels in the channel.

Single event hits can forward bias p-n junctions. The capacitance of a forward-biased p-n junction includes a diffusion term proportional to the gate current. This added capacitance from a semiconductor junction gate gives JFET SRAMs a total device capacitance which is larger than

junctions are forward biased, this condition can not be easily reversed in the JFET due to the large diffusion capacitance component, and recovery depends on the excess minority carrier lifetime in the GaAs.

V_{co} refers to the voltage level required to cause a change of the logic state. The definition of V_{co} is the noise margin (V_{NMl} or V_{NMh}) plus the ambiguous or transition region (reference [126] provides an explanation of static transfer characteristics). The static noise margin can be either the high rail noise margin (V_{NMh} = output high voltage V_{oh} - input high voltage V_{ih}) or low rail noise margin (V_{NMl} = input low voltage V_{il} - output low voltage V_{ol}) depending on a one-to-zero or zero-to-one transition in the cell. The ambiguous region is defined as V_{ih} - V_{il}. Therefore V_{co} can differ from transitions in the cell and also between different technologies. Table 9 shows simulated data for five GaAs memories technology types and shows the voltage level transition

Table 9. SRAM Logic Voltage Data.

Technology	NM_{low}	NM_{high}	V_{dd}	$V_{co(g-d)}$	$V_{co(s-d)}$
C-EJFET	300	598	1.0	402	700
C-EJFET w/resistors	295	399	0.8	401	505
E/D	140	215	0 7	311	386
D-MESFET w/resistors	150	31	3.0 -2.0	970	851

needed for each node in the cell. $V_{co(g-d)}$ refers to the voltage needed at the gate of the hit FET to change the gate node from a logic level zero to a logic level one. $V_{co(s-d)}$ is the voltage needed at the drain of the hit device to cause the drain node to reach a logic level zero from a logic level one. V_{co} can be defined as

$$V_{co(g-d)} = V_{ih} - V_{ss} ,$$

where V_{ih} is the input high voltage, and V_{ss} is the lower voltage supply, and

$$V_{co(s-d)} = V_{dd} - V_{il},$$

where V_{dd} is the higher voltage supply and V_{il} is the input low voltage. The second CMOS line is for a cell with resistors which have been suggested as a hardening approach.

From Table 9 it can be seen that for C-EJFET and E/D MESFET designs the gate voltage transition associated with logic state reversal is smaller than the corresponding drain voltage level transition. Note that these voltage levels are derived from DC noise margin analyses of the memory cells; either the gate or the drain must reach these voltages to initiate the logic state reversal. These data reinforces the concept that gate-to-drain photocurrents can more easily initiate upset than can drain-to-source photocurrents.

For the second term in Equation (3) which represents the charge removed from the node, I_s refers to the static current through the cell and is proportional to the power dissipation of the cell. k defines the fraction of total cell current through the hit node. Charge supplied to or flowing from the hit node during the perturbation contributes to the critical charge; this total charge magnitude equals that collected from the event (i.e. supplied by the photocurrent pulse). Currents supplying drain nodes are limited by the current drive capability of the load devices. Gate currents are dependent on the leakage current of the junction and the junction bias voltage, but gate currents are typically orders of magnitude smaller than load currents. Therefore gate hits require less resupply current to dissipate the excess charge. For large amounts of charge collected at the gate node, the junction becomes forward biased and the magnitude of the gate leakage current is increased. Therefore the $k \cdot I_s$ term for gate-to-drain photocurrents is considerably smaller than for source-to-drain photocurrents during normal biasing conditions. It should be pointed out that a forward-biased gate junction may increase the current available to discharge the perturbed gate node. However, load devices or additional elements (decoupling resistors) may limit this current during a forward-biased condition.

5.4 SEU SIMULATION TECHNIQUES.

Circuit simulation provides a cost-effective method for predicting single event vulnerability without running numerous single event experiments, provided that simulations accurately predict the circuit response to single particles. A SPICE-based GaAs MESFET/JFET model has been used to accurately predict critical charges for several GaAs SRAMs [119, 125, 127]. Future analysis of new device structures (i.e. MODFETs) may require the higher accuracy of 2-dimensional modeling.

The present 1D models are derived from analytical equations and include several important effects particular to modeling SEU in GaAs SRAMs. The model employed considers velocity saturation and pinch-off effects to accurately describe I-V characteristics. Subthreshold region equations are provided to accurately model low power RAM cells. To correlate photocurrents

and critical charge, capacitance equations describing depletion and diffusion capacitance for forward- and reverse-biased cases have been provided in the model. Photocurrents are modeled by exponential current sources or time-dependent resistances, typically with 10 ps rise times, and 250 ps fall times.

Definition of the observation period is important in determining correspondence with SEU experiments [128]. This choice of observation time allows for the simulation of single event disturb errors [129], where under some conditions, the cell may take a long time to recover if the recharging current is small due to a high impedance load. The fast response of typical GaAs devices resolves logic states within 5 ns of the single event hit. Only cells incorporating high impedances to reduce power consumption or to isolate vulnerable nodes are perturbed for longer than 5 ns by a single event; the data in the following table reflects extended observation for these particular cases. Table 10 provides simulation data on three GaAs memory technologies: C-EJFET, E/D MESFET, and D-MESFET/resistor. Figure 42 shows a schematic of a 6-resistor decoupling approach using JFETS. Figure 43 shows a E/D MESFET memory cell including two additional pass transistors (8-T cell). Additional examples of resistive schemes have been examined in other work by these authors [119, 125]. It should be noted that critical charges for source-to-drain upsets have been updated since previous published work due to the change in the method for modeling the source-to-drain charge collection. These results show that gate-to-drain critical charge is the limiting factor in determining the error rate. The results for the C-EJFET cell have been re-evaluated due to recent device capacitance measurements provided by the manufacturer. These modeling changes result in higher predicted critical charges than those previously published.

Table 10. Simulation data for GaAs static memories.

Memory Cell	Supply Voltage (volts)	Noise Margin (mV)	Power Dissipation (μW)	Q_{crit}[a] Gate-Drain (pC)	Q_{crit}[a] Source-Drain (pC)	Error Rate[b] (error-bit/day)	Cell Write Time (nsec)
C-EJFET	0.8	270	1.7	0.054	0.192	3.54×10^{-7}	0.75
C-EJFET Res. Dec.	0.8	215	0.57	0.033	No upset	6.14×10^{-7}	14.0
C-EJFET Res. Dec.	0.8	190	0.62	1.1	No upset	1.74×10^{-7}	17.0
DMESFET /resistor	3.0 −2.0	31	1.3	0.0068	0.0181	3.31×10^{-5}	0.081
Enh/Dep MESFET	0.7	140	44.4	0.0531	0.072	1.46×10^{-6}	0.233
Enh/Dep 8-T cell	0.7	100	44.1	0.105	0.160	6.38×10^{-7}	0.49

Notes:

[a] Q_{crit} is the minimum charge required to upset the memory cell.

[b] The multiplication factor to determine error rates was derived for Si obtained from Reference 16.

Supply voltages for C-EJFET, and E/D MESFET are limited by barrier heights of their respective gate junctions. Other technologies such as D-MESFET/resistor require level-shifting diodes in order to switch depletion driver transistors. Because of the low supply voltages used in these technologies, noise margins are small, typically a few hundred millivolts. Supply voltages above junction barrier heights result in increased gate leakage and, power dissipation and in reduced noise margins.

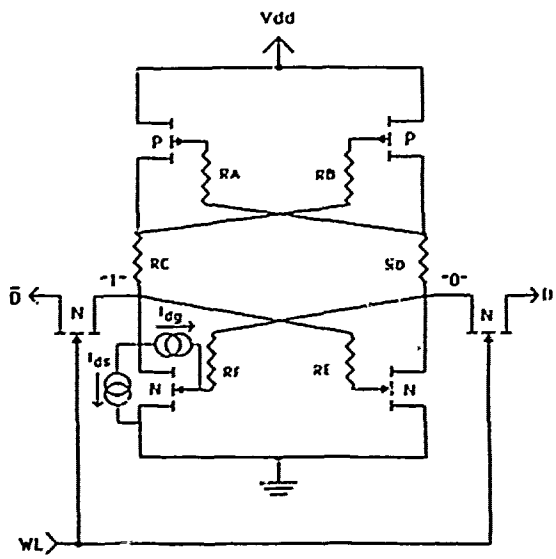


Figure 42. Six-resistor decoupling C-EJFET RAM cell.

Simulated critical charge data has agreed very well with the available experimental data [125]. Values simulated for several hardening approaches are also provided, along with estimated soft error rates and memory cell write times. Soft error rates are calculated using Equation (1).

Simulation of local memory write times (not including peripheral circuits) are included to provide estimates of the effects of hardening approaches on memory speeds.

5.5 HARDENING TECHNIQUES.

Hardening techniques can be employed at either the device technology or circuit level of the memory design. Device technology techniques, such as buffer layers, or p-implants, can be used to reduce the effects of funneling, and decrease collection volume dimensions [130,131]. The use of insulated gate structures (MISFETs) in GaAs technologies may eliminate the vulnerability to gate hits. However no reliable MIS technology has yet been developed for GaAs. Recent advances in heterojunction gate GaAs technologies such as HIGFETs and MODFETs may also reduce the sensitivity to gate hits.

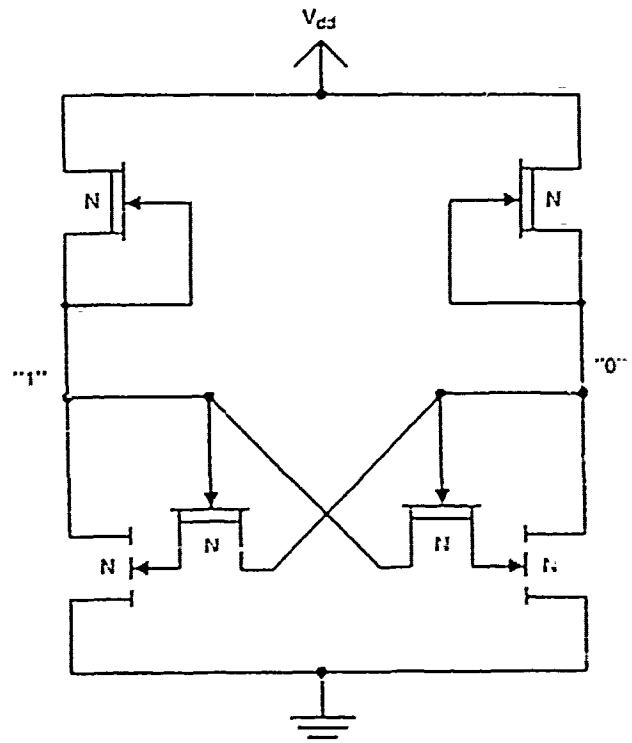


Figure 43. Eight-transistor E/D MESFET cell.

Circuit hardening techniques use additional circuit elements to isolate hit nodes from information storage nodes. The use of resistors to decouple gate nodes from source-to-drain photocurrents in CMOS memories has decreased soft error rates by several orders of magnitude [132]. Several techniques to harden against single events in GaAs SRAMs have been examined in this work, including resistive and active decoupling approaches [125]. Resistive techniques applied to C-EJFET simulations show that source-to-drain critical charge can be increased into the picocoulombs range, but at the cost of increases in memory write times (see Table 10) [124]. The only effective method for hardening against gate hits with decoupling resistors is to isolate the perturbed devices by large impedances. This approach is only effective against gate hits when the cell's intrinsic time constants are larger than time constant of the perturbed device. This hardening philosophy can be illustrated by making the observation time, t_I of Equation (3), a large value. The second term on the right hand side of Equation (3) then becomes proportional to t_I (if I_s remains constant over most of the observation time). To obtain an increase in gate-to-drain critical charge for a C-EJFET cell incorporating 150-kΩ decoupling resistors, an observation time on the order of 100 ns is required. This extended observation time corresponds to an extended minimum interval between successive read operations, i.e. to a reduction in the memory's assess speed and write times. Resistive decoupling techniques have been applied to

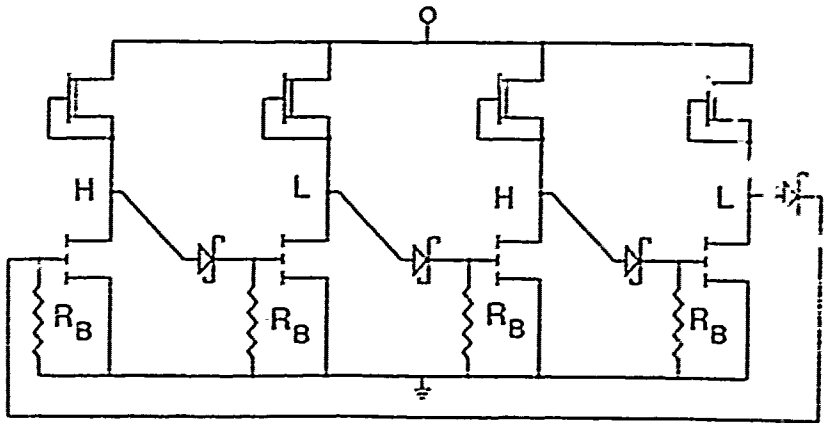
complementary E-JFET memories, where memories have shown upsets to heavy ions but not protons [118], but write-time performance on these modified devices has not been reported. Simulated local write times suggest periods on the order of tens of nanoseconds. This increase in write times would remove the GaAs SRAM's speed advantage relative to silicon SRAMs.

Another circuit approach is to use active devices instead of resistors within the memory cell (Figure 43). Depletion MESFETs can decouple the gate nodes from the source-to-drain photocurrents, yet allow a discharge path for charge collection on gate nodes. Simulations have shown that gate-to-drain critical charge can be increased by 100%, without substantially degrading cell write times. However, noise margin is reduced by 28%, and a considerable increase in cell area (approximately 33%) is required to implement the devices. The use of additional devices in the memory array may reduce yield.

It is possible to use local information storage redundancy to harden GaAs RAM cells [134]. One such circuit using four inverter stages is shown in Figure 44 using enhancement-depletion mode stages. In this cell, SEU hardness is achieved at the expense of a more complex cell design. In steady state the four stage inverter chain has two high logic nodes and two low logic nodes. A particle hit on any one of the devices with a high logic node will not destroy the high logic state of the other high node. The Schottky diodes are required to isolate the hit transistor drain from the succeeding gate while the drain recovers from an SEU event. The upset threshold of the RAM cell is determined by the value of resistor R_B which may also be replaced by a depletion mode FET. SPICE simulations have verified that this type of cell can achieve a critical charge of several pC depending on the value of R_B[134].

Two cross-coupled inverter stages connected in a hard wired OR configuration as shown in Figure 45 can provide even greater SEU hardness. In this circuit the R_B resistors of Figure 44 have been replaced by depletion mode FETs. This design is somewhat complex requiring eight Schottky diodes and 12 FETs. Additionally four access transistors (not shown) are required to read and write to the cell. This cell, however, can be designed to be radiation hard with little speed penalty in read/write time. The cell is basically two conventional RAM cells in an OR connection such that a logic state reversal at the collector of any one of the stages will recover without upsetting the logic state of the other inverter pair. The high state of both invertor pairs must go low before the cell will switch states. SPICE simulation of the design of Figure 6 with typical 1μm design rules have demonstrated no upset with source-to-drain current sources and a critical charge of greater than 12.5 p Coul for a gate-to-drain hit.

The use of local cell redundancy techniques such as shown in Figures 44 and 45 are the only presently known circuit level hardening techniques for GaAs RAM cells. Such complex circuits are required by the drain-to-gate induced charge in GaAs devices which is not present in silicon MOS devices. It is interesting that the OR hardening approach does not work with a complementary GaAs FET approach. This is because the hardening approach depends on the SEU particle only causing high nodes to go low. With a complementary technology an SEU event can also cause a low node to go high and the OR configuration does not work.



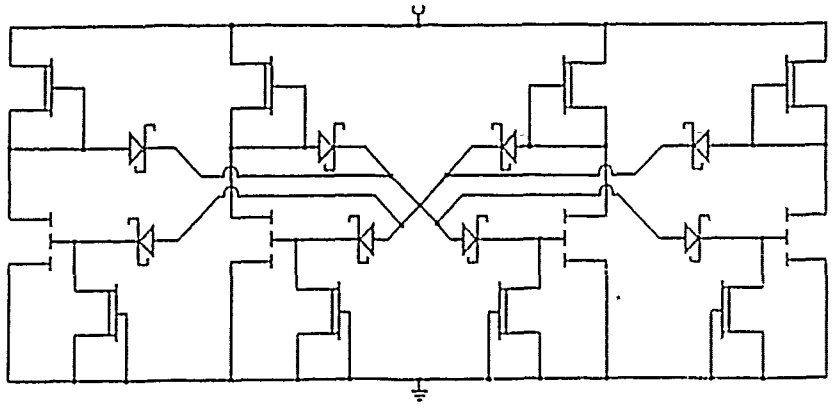
R_B may be replaced by a depletion mode FET

Figure 44. Hardened E-D GaAs FET cell, using local information redundancy and enhancement-depletion mode stages.

5.6 CONCLUSION

Presently, no one particular GaAs technology has a clear advantage in terms of SEU tolerance. Values for the critical charges of unhardened GaAs SRAMs from both simulations and experiments are in the range of 50 fC [117]. These values are considerably below these of present hardened CMOS memories primarily because the small GaAs device feature sizes result in smaller circuit capacitances and correspondingly smaller voltage swings in response to single-event induced currents. Unhardened silicon memory designs with feature sizes comparable to those of present GaAs memories, (i.e. 1 um gate lengths) are expected to have comparable critical charges [119, 133].

The small gate-to-drain critical charges (20 fC to 50 fC) are the primary factor limiting the reduction of error rates in GaAs SRAMs. Gate vulnerability is not eliminated by the use of the cross-coupled feedback resistors used in hardened CMOS designs. Larger device geometries reduce the error rate but the concomitant increased capacitance degrades operating speeds and increases power dissipation, making GaAs hardening by this method undesirable with a high speed technology. Circuit hardening techniques can be employed, but tradeoffs for noise margin, write times, power dissipation, cell area, and SEU vulnerability must be examined. The compromises incorporated in single event hardened designs will determine if such GaAs memories retain advantages to system designers. If so, future GaAs SRAMs may be designed with SEU hardening as a primary design consideration.



Gate-to-Drain Critical Charge = > 12.5 pC

Power Diss. = 355 mW @ 2.0 V

Source-to-Drain Critical Charge = no upset

Noise Margin = 96 mV

Figure 45. Hardened GaAs E/D cell with ORed configuration.

SECTION 6

BIPOLAR SINGLE EVENT EFFECTS

6.1 INTRODUCTION.

The vulnerability of a given memory cell to SEU is dependent on a number of material, device and circuit level parameters. The most critical of these are the amount of charge collected at a particular circuit level node and the capacitance associated with the circuit. The circuit level capacitance in turn is intimately related to the speed of the memory cell. Fast Bipolar RAM cells require small geometries with small capacitances and such cells are particularly vulnerable to SEU.

The increased power dissipation of bipolar RAMs over MOS or CMOS RAMs, favors the use of MOS RAM cells except in applications requiring the high speed of the bipolar RAMs. Because of several factors, which are subsequently discussed in more detail, bipolar RAM cells are especially susceptible to SEU effects. The purpose of this work is to present a review of SEU effects in bipolar RAM cells and SEU hardening approaches. Included are a discussion of the basic physical processes of SEU, a discussion of circuit level modeling of bipolar SEU effects, some conclusions regarding the general sensitivity of bipolar RAM cells to SEU and hardening approaches.

6.2 BASIC SEU PROCESSES IN BIPOLAR DEVICES.

In order to understand SEU effects fully, it is necessary to examine the problem at several different levels including the basic device level, the circuit level and finally the system level. At the basic device level one is concerned with the interaction of the charge created by a high energy particle with the basic p-n junctions present in the device. Figure 46 shows a basic cross-section of an npn transistor in IC form and possible paths of a high energy particle through the device. These paths are of course only representative and particles may penetrate the structure at any angle.

For typical device dimensions and particle energies of interest, the particles penetrate completely through the active device regions consisting of the p-n junctions. This is illustrated by Figure 47 which shows the production rate of excess electron-hole pairs along the path length in silicon for two particles, one a 2.88 MeV He ion and the other a 57.3 MeV Cu ion. Although one of these is a low-energy light ion and the other a high-energy heavy ion, both particles have path lengths which exceed 10 μm in silicon. This penetration depth is typically much deeper than the depth of the p-n junctions for bipolar transistors as seen in Figure 46.

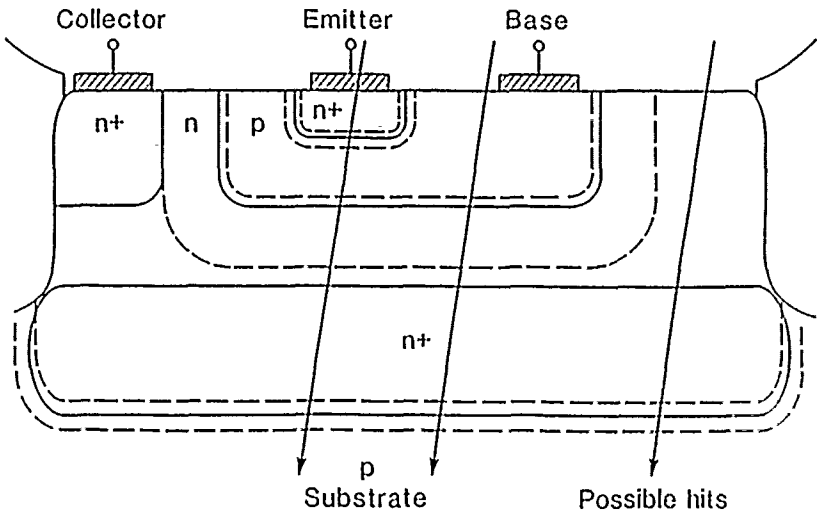


Figure 46. Bipolar transistor cross-section showing three possible paths for a high-energy particle.

Figure 47 also illustrates the fact that the charge generation rate may have a maximum near the end of the track, as for He, or may steadily decrease, as for high energy Cu. For shallow devices (of only a few μm in depth) a uniform generation rate along the track interacting with the device may be taken as a reasonably good approximation. The charge initially produced along the track consists of course of equal densities of electrons and holes and Figure 47 shows the generation rate for the positive hole charge. In silicon, an excess electron-hole pair is generated for each 3.6 eV of particle energy loss. The volume density of generated carriers depends on the radial size of the track which is not completely known. However, estimates of an initial track radius of around 1000 Å can lead to initial track densities as high as 10^{20} - $10^{21}/cm^3$, and this can exceed the doping density in many device regions within a thin tube along the ion track.

Following an ion hit in a transistor structure such as shown in Figure 46, charge is separated by the junctions and appears as current pulses at the various transistor nodes. A good first-order approximation to the charge collected by any transistor junction is to assume that all the charge generated within the junction depletion region and one-half the charge generated in the neutral regions between the depletion regions will be collected by the p-n junction. The depletion region boundaries are illustrated in Figure 46 by dotted lines. Such a simple approximation is possible in a bipolar transistor structure because the distances between the depletion regions is typically much less than a diffusion length and very few carriers are lost by recombination. An exception to this simple view is the substrate buried layer (n^+ in Figure 46) junction. Since the substrate is very thick compared to a diffusion length, one must account for carrier loss by recombination in the substrate in evaluating the isolation junction current.

Typical junction carrier collection depths in silicon bipolar devices range from about 0.1 μm to 1.0 μm. Thus one can estimate that the 57.3 MeV Cu ion shown in Figure 47 would result in a junction charge of 30 - 300 f coul while the 2.88 MeV He ion would result in only 1-10 f coul of charge at the transistor nodes.

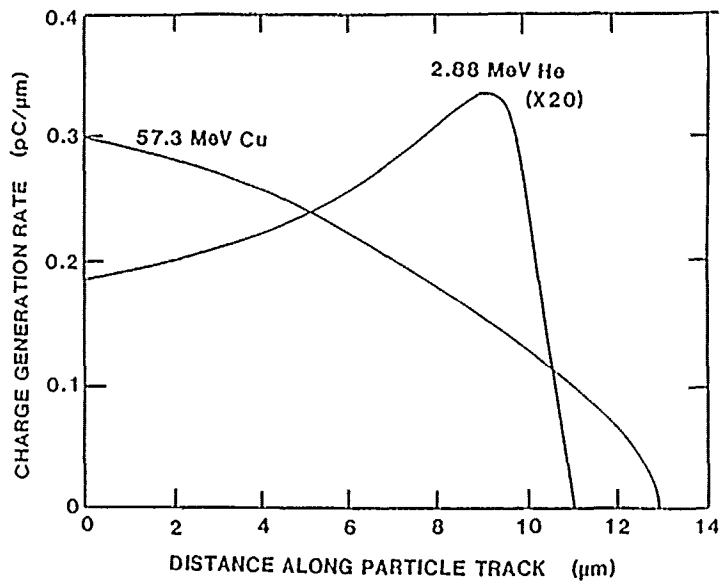


Figure 47. Charge generation rate in silicon for two particles.

In addition to the total collected charge, the time profile of the collected charge is important in determining the circuit level effects of a particle. Two time constants are typically identified with the charge collection process. The first is the prompt charge collection phase while the depletion region charge is collected by the junction and the depletion region recovers. The second is the longer time associated with the diffusion of carriers to the junction depletion region. This simple picture is complicated when the carrier density exceeds the background doping density and the depletion region is greatly distorted leading to the funneling effect [135-139] with single junctions and an ion shunt-like effect across multiple junctions [140-142].

Considerable experimental and theoretical work has been done on the time profile of the collected charge. For SEU, the fast prompt charge is of most importance, since circuits can respond to a slow current pulse by supplying charge from the external power supply. The rise time of the prompt current is believed to be in the psec range while the fast phase of the charge collection is generally believed to have a time constant of a few tenths of a nsec to at most a nsec. In modeling circuit-level SEU effects, a specific time profile is usually assumed such as a fast rising exponential followed by a slower exponential decay. Computer simulations to be discussed later have used a current of the form

$$i(t) = i_{max} \left[\exp(-t/\tau_f) - \exp(-t/\tau_r)\right], \qquad (1)$$

where τ_r and τ_f are the rise and fall times of the current pulse.

The total charge and the time profile are known to depend somewhat on the voltage across a p-n junction. Most first-order considerations of SEU effects in bipolar or MOS circuits do not take this into account. If the total collected charge can be accurately estimated, then the maximum current (in Eq. (1) for example) can always be adjusted to agree with known results. In bipolar circuits, the voltage dependence of collected charge is expected to be less important than that for isolated p-n junctions or for MOS devices, since essentially all of the charge generated between the surface and the isolation junction will be collected by one or another junction in the transistor.

Although it is important in modeling the transient upset of bipolar transistors to have a model for the time dependence, calculated results do not depend strongly on the assumed time constants. The major reason for this is the fact that the circuit level time constants tend to be larger than the prompt charge collection time constants. In this case the important quantity is the total charge deposited on the circuit nodes and the effect can be characterized entirely in terms of a total charge needed to upset the circuit. This point will be discussed in more detail in a later section of this work.

6.3 BASIC BIPOLAR RAM CELLS.

Bipolar RAM cells are typically based on one of three circuit level configurations. These are (1) Emitter coupled logic (ECL) cell, (2) Schottky logic cell or (3) Integrated Injection logic (I^2L) cell. The basic RAM configurations are shown in Figure 48 without the complications of row and column address circuits. As with most applications, there are various tradeoffs among the different RAM cells. The Schottky based cell has the largest number of components but is a non-saturating cell which offers the highest speed. The I^2L cell on the other hand offers low power operation at a slower speed and is easily programmed over a wide range of speeds by increasing the power level. The ECL based cell, is simple in design and has somewhat intermediate speed-power properties between the other cells.

It should also be noted that a common practice in bipolar RAMS is to "power down" the cells when they are not being addressed for read or write in order to reduce power consumption. For example, with the ECL cell (Fig. (48a)) the value of V_{cc} might be 5V during a read or write operation on the cell. This might then be reduced to a steady state condition of 1.0 - 2.0V, which is sufficient to retain the stored information but which gives a greatly reduced stand-by power. This provides the advantage of lower power without a large speed penalty. However, the RAM cells can be considerably more vulnerable to SEU in the low power state.

Another significant difference between the cells is the magnitude of the logic level swing. For the Schottky cell, the collector voltage swings from V_{cc} in the high state to a low level equal to a collector saturation voltage (0.1 - 0.2V). For the ECL and I^2L cells, the logic level swing is from a diode "on" voltage (0.6 - 0.7V) to a collector saturation voltage. The logic level swing is thus much larger in the Schottky cell and this is advantageous for improved SEU response.

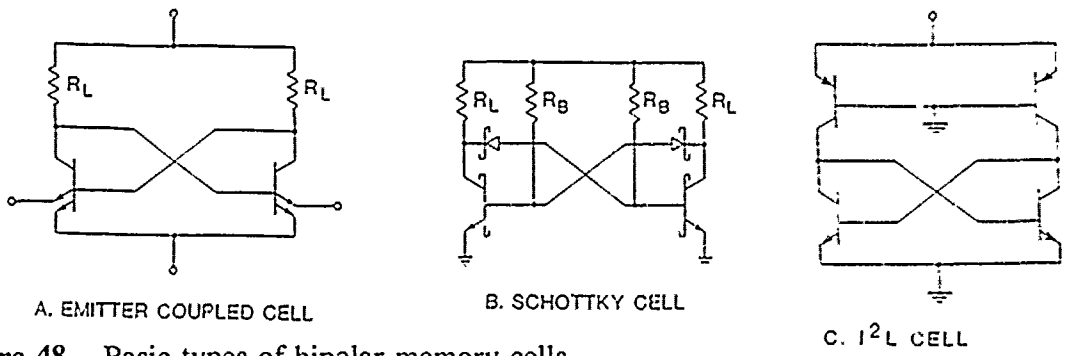


Figure 48. Basic types of bipolar memory cells.

The circuit level device parameters associated with a particular RAM cell are to some extent technology dependent. For example the device capacitances depend on the transistor doping levels, junction areas and isolation techniques. In recent years considerable improvements have been made in bipolar technologies by using self-aligned structures including oxide isolation techniques for the side walls of the transistors. These techniques have contributed to higher speed devices by reducing device dimensions and reducing parasitic capacitances. Spratt and Torrence [148] have given typical circuit level device parameters for a TI 2.0 μm technology. These are shown in Table 11 and have been used in this work as typical of a present day advanced bipolar transistor technology. The most important feature of the data is the very small capacitance values which are desirable for high speed but which can lead to a low threshold for SEU.

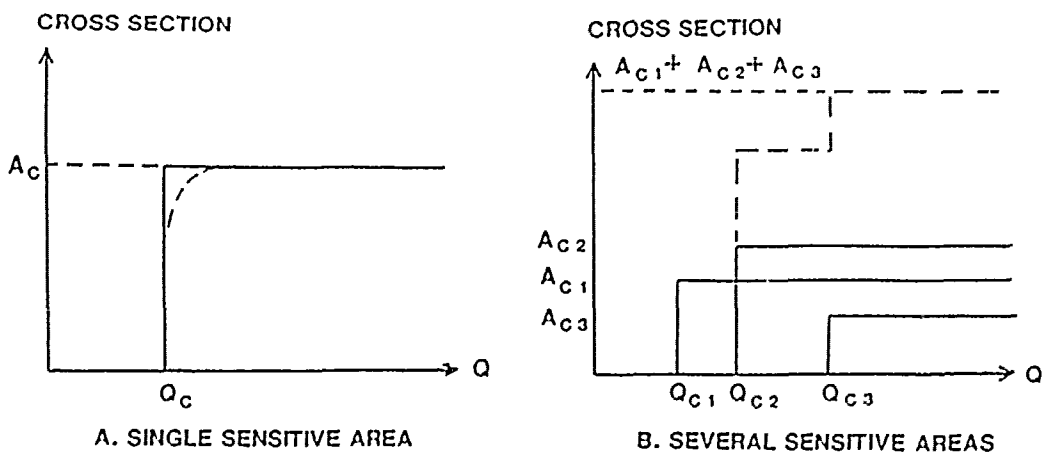


Figure 49. Illustration of ideal RAM cell upset cross sections.

TABLE 11. Typical IC and device parameters for a 2.0 μm silicon bipolar technology.

DC PARAMETERS

Parameter	Value
DUF (Buried-Layer) Resistance	15 Ω/□
Epitaxial Layer Thickness	1.0 μm
High Sheet Resistance	2,000 Ω/□
Pt Sheet Resistance	300 Ω/□
h_{FE} dc current gain	100 typical
BV_{CBO}	20 V
BV_{EBO}	6.5 V

SPICE PARAMETER

Parameter	Value
C_{BC} (Base-Collector Cap.)	0.04 pF
C_{CS} Collector-Substrate Cap.)	0.06 pF
C_{BE} (Base-Emitter Cap.)	0.02 pF
T_F (Forward Transit Time)	40 psec.
R_B (Base Resistance)	700 Ω
R_C (Collector Resistance)	150 Ω
R_E (Emitter Resistance)	4 Ω

6.4 MAJOR FACTORS DETERMINING SEU.

SEU for RAM cells is typically characterized by two parameters which are critical charge for upset and upset cross-section. An ideal SEU response [illegible] is shown in Figure 49(a) where every particle which deposits a charge of Q_c or above [illegible] sensitive area A_c causes a memory cell upset and loss of information. Relating [illegible] 46, the area might be the collector-substrate isolation region and every particle [illegible] this area and depositing Q_c within the junction collection distance would cause an upset.

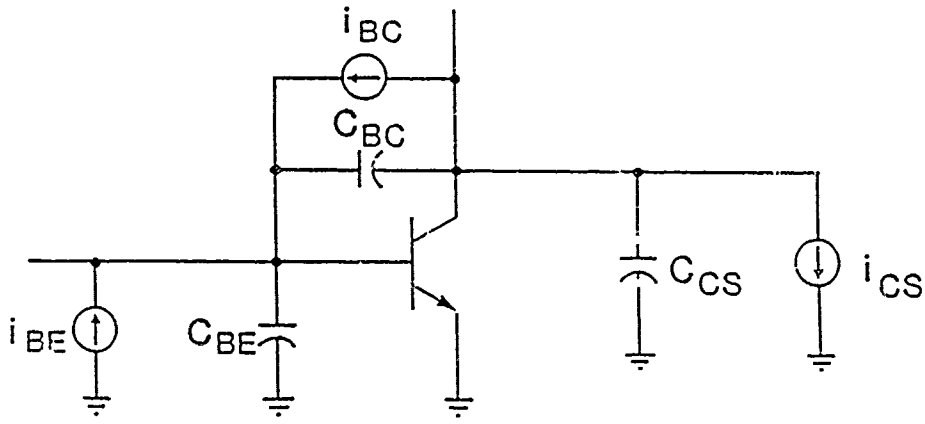


Figure 50. Isolated transistor illustrating circuit-level current sources and device capacitances.

These ideal concepts were initially developed for MOS and CMOS RAM cells where there tends to be one major sensitive area and one upset cross-section. The situation is more complicated with bipolar RAM cells, since there are many sensitive areas with potentially different charges required to cause an upset. For example in Figure 46, one can easily identify three separate areas for hits through the emitter, (and base and collector) through the base (and collector) and through the collector. The minimum deposited charge required for an upset may be different for each of these areas and this leads to an upset cross-section curve as shown in Figure 49(b). Actual experimental data typically shows some rounding of the curve as shown by the dotted line in Figure 49(a). This can arise from a distribution of Q_c values over a large numbers of RAM cells even when there is only one critical area.

Figure 50 shows a somewhat simplified version of a bipolar transistor with the device capacitances explicitly shown and with current sources across all junctions to simulate collected charge due to potential ion hits at any of the junctions. The current source i_{cs} for example represents current collected by the collector-substrate junction. For an *npn* transistor, the

directions of the currents are as indicated, with both the emitter-base (i_{BE}) and collector-base (i_{BC}) currents tending to forward bias the transistor junctions. For a particle hit through the emitter, all three current sources would be present.

The current sources i_{BE} and i_{BC} act in a fundamentally different way from i_{cs} in causing a RAM cell upset. If the transistor in Figure 50 is initially off, the base voltage will be low and the collector voltage high. (Other components needed to complete a memory cell are not included in Figure 50 to simplify the picture). Currents i_{BE} and i_{BC} tend to drive the base node high and correspondingly the collector node low. If the base voltage change is sufficiently large, a logic state reversal will occur at the transistor and if this gets coupled to the other RAM cell transistor before the node can recover, an SEU has occurred.

The current i_{cs} acts in a different manner to cause an upset. This current pulls the collector low and this in turn is coupled to the other side of the memory cell causing the opposite transistor which was initially on to turn off. This causes an SEU when the high voltage from the opposite side then gets coupled back to the struck transistor turning it permanently on.

If a transistor which is already on with its base high and collector low is hit by an ion, the current sources all tend to reinforce the logic state and no upset occurs. Thus only the off transistor in a RAM cell pair of transistors is at any given time sensitive to logic upset. For bipolar devices one would expect to have at least three major cross-sections and three critical charges corresponding to the three different hit locations as shown in Figure 46. Somewhat intuitively, one would expect the critical charge to increase in the order of emitter hits, base hits and collector hits while the cross-sectional area increases in the same order.

Although the details of an SEU upset are somewhat complicated by the actual RAM cell circuit, reasonably accurate first-order approximations to the critical charge can be made relatively easily. If one neglects in Figure 50 any charge which flows into or out of the transistor from other parts of the RAM cell, then one can calculate the change needed to change the voltages as

$$\Delta Q = C_{BE}\Delta V_{BE} + C_{BC}\Delta V_{BC} + \tau_F \Delta I_C \qquad (1)$$

where $\tau_F \Delta I_C$ is the charge storage within the device which is needed to drive the collector to saturation. For a 0.1mW cell operating at 2V we can estimate $\Delta I_C \approx 5 \times 10^{-5}$ amp and for a typical τ_F of 40 psec one obtains $\tau_F \Delta I_C$ small for low power RAM cells and will be neglected to first order.

For a logic state reversal $\Delta V_{BC} = 2\Delta V_{BE}$ and

$$Q_{BO} \sim (C_{BE} + 2C_{BC})\Delta V_{BE} \ . \qquad (2)$$

For the parameters of Table 11 and a $\Delta V_{BE} = 0.3V$, this gives a Q_{BO} of about 30 fCoul. This represents a lower limit to the critical charge since any charge which flows to other parts of the cell will decrease the charge available to change the emitter-base voltage in Figure 50. Also, any charge which flows from the power supplies during the time of the current pulse tends to stabilize the circuit and increase the critical charge.

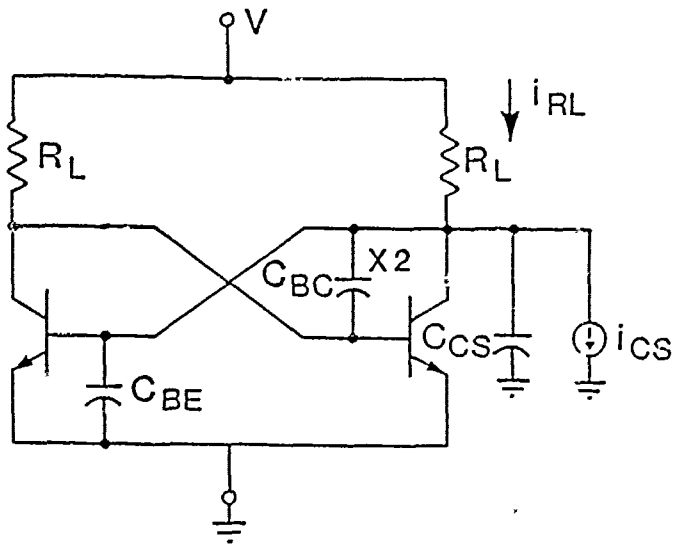


Figure 51. Illustration of ECL RAM cell with capacitances at collector node.

In a similar manner, the charges associated with a collector-substrate hit can be estimated from Figure 51. In this case only the capacitances directly associated with the collector node are shown. Again neglecting transistor charge storage and taking $\Delta V_{BC} = 2\Delta V_{BE}$ one obtains

$$Q_{CO} \sim (C_{BE} + C_{CS} + 4C_{BC})\Delta V_{BE}, \qquad (4)$$

and using the same values as before gives

$$Q_{CO} \approx 50 fCoul.$$

While these estimations are based upon a very simple model, they provide the correct order of magnitude estimations of critical charge and also predict that the critical charge for a collector-substrate hit should be larger than that for the emitter hit.

The first order effect of finite current flow from the power supply can be included by considering the current i_{RL} in Figure 51. The current source must supply the charge needed to change the capacitor voltages and must also supply the current through R_L before the logic state reversal becomes latched into the memory cell. This can be included in the model for critical charge as

$$Q_c = Q_{co} + I_A T_w \,, \qquad (5)$$

where T_w is the upset current pulse width and I_A is the average current through the load during the pulse. Estimating this as V_{cc}/R_L gives

$$Q_c \approx Q_{co} + \frac{V_{cc} T_w}{R_L} \,. \qquad (6)$$

This simple equation illustrates several important concepts with regard to critical charge in bipolar RAM cells. First, the concept of a critical charge which is independent of pulse shape and pulse width is valid as long as the charge supplied to the device from the external power supply during the pulse width is negligible compared with the SEU charge. This tends to be a much better approximation for MOS or CMOS RAM cells than for high speed bipolar RAM cells. The correction due to a finite pulse width can in many bipolar RAM cells be as large as the intrinsic critical charge. This of course improves the cell with respect to SEU. This relationship also illustrates that critical charge can be increased at the expense of increased power dissipation by decreasing R_L.

This section has discussed first order circuit-level SEU effects and developed rather simple first-order approximations to the critical charge for bipolar RAM cells. The major dependencies of the critical charge have been verified by more detailed computer simulations to be discussed in the next section. At first it is somewhat surprising that the critical charge does not depend on other device parameters such as bipolar transistor gain, since the device can amplify a current appearing at the base, and give a much larger collector current. While this is true and the charge which flows between collector and emitter can be much larger than the charge which flows into the base, the transistor can not generate additional charge. Only the current due to

the incident particle gives a charge which can change the capacitance voltage levels on a time scale faster than the circuit level time constants. This relative independence of transistor beta has been verified by computer simulations where the beta for a ECL like cell was varied from 1 to 1000 and the critical charge changed only by about 20%. Computer simulations also verify that the critical charge scales approximately linearly with the circuit level capacitance values.

6.5 SEU MODELING AND RESULTS.

Computer circuit level simulations are needed for a complete characterization and evaluation of bipolar SEU effects. In this work this has been done by using SPICE at the circuit level with the SEU charge represented by an exponentially shaped pulse as previously discussed. Typical rise time was taken as 10 psec and the current decay time was varied from near zero to 1 nsec but was typically taken as 0.25 nsec.

Integrated circuit transistors are more complicated than the simple lumped models discussed in the previous section. Because a particle strike is a very localized event, the two-dimensional nature of the transistor is important in determining SEU effects. A distributed model of the transistor as shown in Figure 52 has been used to model the base and collector regions. The lumped ideal transistor in Figure 52 models the region in Figure 1 directly under the emitter.

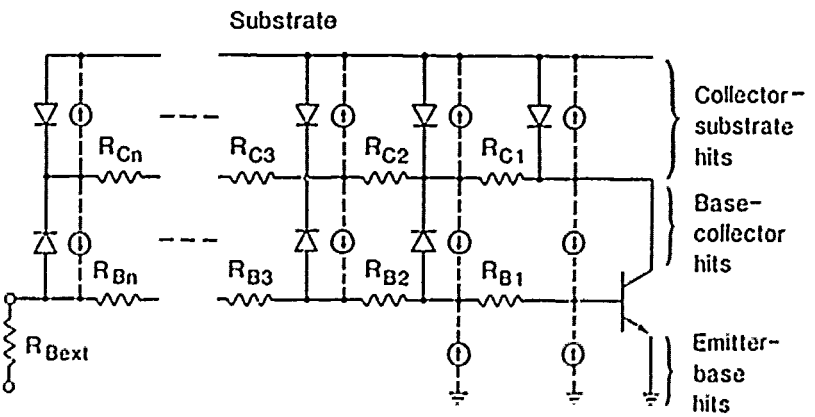


Figure 52. Distributed model of bipolar transistor used in computer simulations with possible current sources due to particle hits.

Current sources are shown in Figure 52 to represent particle hits either close to the emitter or somewhere between the emitter and the external base contact. Because of the distributed base resistance, the critical charge depends on how far from the emitter junction the hit occurs. The distributed transistor model with typically 4 or 5 sections used to represent the base has been

used with a lumped parameter description of the load resistors and layout capacitances. To determine critical charge at the various nodes, transient simulations are performed with increasing levels of integrated charge. The transient node voltages are observed and the cell can be determined either to upset or not upset.

Calculated critical charges for such a Schottky RAM cell are shown Figure 53 as a function of the assumed current pulse decay time constant τ_f. The circuit level device parameters used in this simulation were not exactly those shown in Figure 49 but were reasonably close to these values. A range of values is shown for a base hit with the smallest Q_c values corresponding to a hit through the emitter and the largest values corresponding to a hit in the base region near the base contact. Curves are also shown for a collector-substrate hit illustrating the larger critical charge for such hits. For pulse time constants larger than about 0.5 nsec, the critical charge is seen to vary approximately linearly with pulse width as predicted by Equation (5). The minimum critical charge for a hit on the emitter with a time constant of 0.25 nsec is seen to be about 50 fCoul and this increases to about 200 fCoul for a collector-substrate hit. These detailed simulation results are within a factor of 1-4 of the results calculated using the simple method of the previous section. The difference in Q_c between a collector-substrate hit and the emitter or base hit is larger in this Schottky case than one would expect in the case of an ECL RAM cell because of the larger collector voltage swing of the Schottky RAM cell.

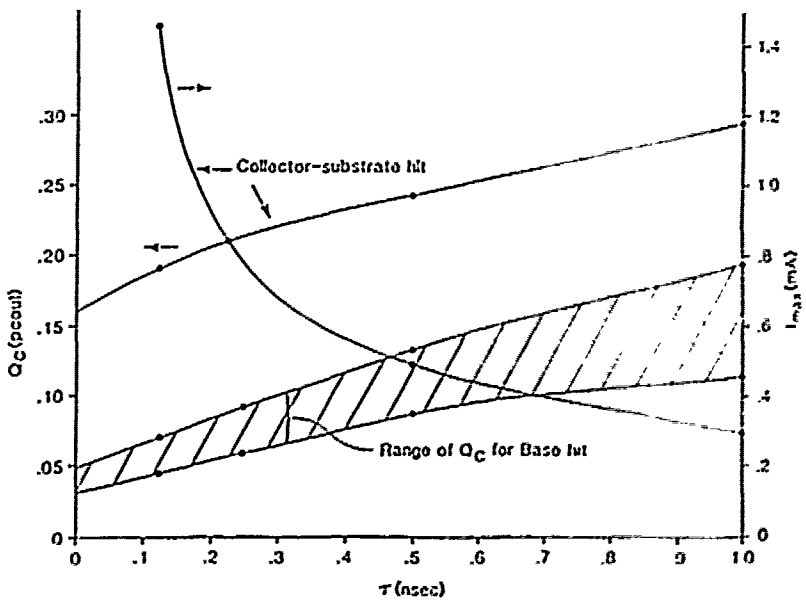


Figure 53. Illustration of the dependence of critical charge on time constant of charge-collection process for Schottky RAM cell.

The most extensive expermental data on critical charge and upset cross-section is the work of Zoutendyk, et al. [143, 144] and the results of their work are shown in Figure 54. This data is for a Schottky ECL type RAM cell and data were taken in both the power-down (U points in

Figure 54) and the power-up read/write mode (A points in Figure 54). Consider first the power-up mode with the square data points. Several breaks and plateaus can be seen in the cross section corresponding to several sensitive areas with different critical charges. Zoutendyk, et al. were able to identify the plateaus on the data with the emitter area (A_E) the base area (A_B) and the base plus Schottky contact area ($A_B + A_{sc}$). In this manner critical charges ranging from 0.5 pCoul to 1.1 pCoul were identified with the various areas. In addition, the transition between the emitter and base area is soft indicating a range of hit locations and corresponding range of critical charge as previously discussed.

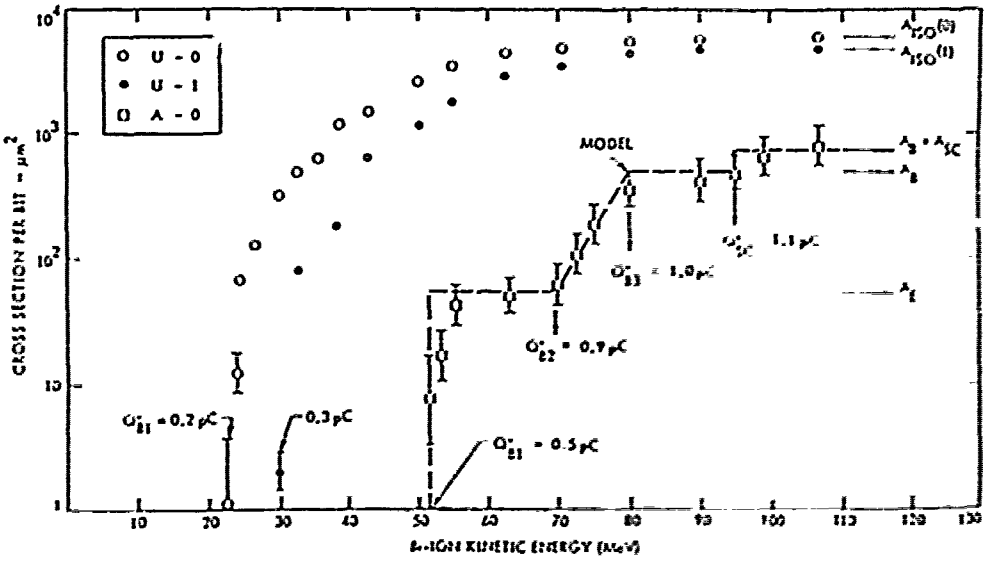


Figure 54. Experimental data on critical charge and upset cross section for an ECL-type RAM [143, 144].

In the power-down state the critical charge was reduced considerably to the range of 0.2 - 0.3 pCoul and showed a soft transition to a total cross-section corresponding to the isolation junction area. At this point the total transistor area is sensitive to a particle hit. The critical charges in this figure are larger than those previously discussed for a 2.0 μm technology because the expermental RAM cells studied were an older technology with a large line width and larger device capacitances. For example, the isolation junction area was around 5,000 μm^2 . These are about an order of magnitude larger than corresponding values for a 2.0 μm technology.

The major factors determining critical charge and upset cross-section for bipolar RAM cells are now reasonably well understood. The major factors determining critical charge can be summarized as:

(1) The circuit level nodal capacitance

(2) The logic voltage swing at the nodes

(3) The intrinsic circuit level time constant relative to the SEU current pulse time constant.

It is interesting to compare the critical charge of bipolar RAM cells with that of other technologies such as NMOS and CMOS. This is shown in Figure 55 where calculated results for 1.25 μm ECL and I^2L bipolar RAMs are shown compared to experimental results collected by Petersen [145]. It is very interesting and important that all technologies appear to give a critical charge Q_c which varies as l^2 where l is the minimum critical feature size, such as channel length. This means that one is dealing with a fundamental physical issue in the critical charge values and, as previously discussed, this is being determined primarily by device nodal capacitance values which scale as l^2.

The critical charge Q_c is one of the important factors determining error rate in bipolar RAMs. Other geometrical factors determining the upset rate can be seen from Petersen's approximation of [149] where R is the error rate (in errors/bit · day), ab is the cross-sectional area in (μm^2)

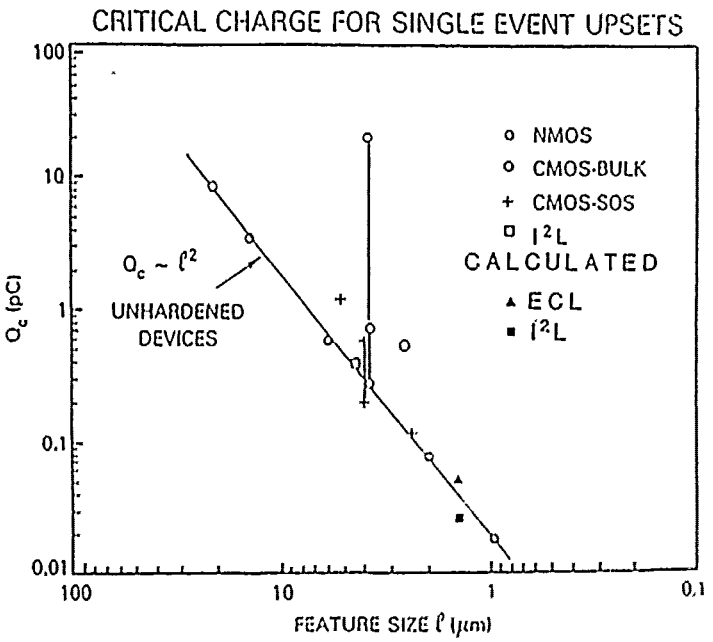


Figure 55. Dependence of critical charge on feature size for different technologies.

$$R=(5x10^{-10})ab(c^2/Q_c^2), \qquad (7)$$

and c is the charge collection depth (in μm). An estimation of R is complicated in bipolar RAMs by the presence of several sensitive areas each with a critical charge. Equation (6) must be applied to each sensitive area and the results summed to obtain a total error rate.

At least three major sensitive areas can be identified with bipolar transistors and associated with particles which penetrate the emitter area, the base area or the collector-substrate area. Each of these can be seen in Figure 54. Q_c is typically smallest for an emitter area hit and largest for a collector area hit. On the other hand the areas vary in the opposite order and the collector area (or collector-substrate isolation junction) typically makes the largest contribution to the total error rate. For a 2 μm line width geometry, the emitter area would be only a few μm^2 while the base area would be 5-10 times the emitter area and the collector area 10-100 times the emitter area. Exact values depend upon the particular technology employed and especially on the use of oxide sidewall isolation techniques for self-aligned device structures [148]. SOS or SIMOX technologies can eliminate the collector-isolation junction and greatly reduce the SEU error rate.

It is sometimes stated that bipolar RAM cells are more susceptible to SEU than CMOS RAM cells. This is more a matter of perception than reality. Bipolar RAM cells are typically employed in systems which require their speed advantage over CMOS RAMs. This means that bipolar RAMs tend to be optimized for speed with small geometrics and low capacitance values. For a given critical feature size, Figure 55 implies that there will be little difference in critical charge between different logic families. Differences between bipolar RAMs and CMOS RAMs must arise primarily from differences in device areas and charge collection depths. The other advantage of CMOS is that present technologies at 3-5 μ line widths can be hardened to SEU by circuit level techniques such as cross-coupling resistors [146,147]. It is not clear that 1-1.25 μm bulk CMOS can be hardened with the same techniques without an unsatisfactory loss in speed. However, new approaches such as SOS and SOI may be hardened without loss in speed.

6.6 BIPOLAR HARDENING APPROACHES.

The major factors determining SEU error rate can be seen from Equation (7). To reduce the error rate one obviously wants to minimize the sensitive area, increase the critical charge and decrease the charge collection depth. In terms of these parameters, hardening approaches can be discussed at either the technology level or at the circuit level.

At the technology level there is an obvious advantage to having c as small as possible, since a reduction in c by a factor of 10 gives a 100 fold decrease in the error rate. The most promising technology approaches for decreasing c are to use some type of silicon on insulator approach such as silicon on sapphire (SOS) or implanted insulators (SIMOX) which give a very thin

silicon over insulator layer. Bipolar RAMs will benefit equally with CMOS by the development of a practical SOI technology. With such technologies, c can be reduced by factors on the order of 10 or more.

At the circuit level, Q_c scales linearly with device capacitance. In most cases it is not practical simply to scale the capacitances since this reduces the speed of the RAM and the major interest in bipolar RAMs is for very fast memory. As previously discussed, Q_c can also be increased by increasing the circuit power level but again this is very undesirable at the system level.

Another circuit level approach is to use some type of delay or charge storage element in the RAM cell feedback path as illustrated in Figure 56. This approach has been very successful with CMOS where a simple decoupling resistor can harden circuits at the 3-5 μm line width level. Such a simple resistor or resistor-capacitor decoupling approach will not work with bipolar cells because of the base current which flows across the feedback path. Adding resistors in fact has the opposite effect of decreasing the critical charge.

Without discussing specific proposals for feedback elements some general conclusions can be drawn about such approaches to bipolar RAM cell hardening. The purpose of the feedback delay or charge storage is to delay a drop in collector voltage on the hit transistor from appearing at the base of the opposite side of the cell by some time interval during which the hit transistor can recover and the logic state reversal will not become permanent. Actually, two delay paths are present between the collector and base of a hit transistor. In order for this scheme to work the delay must thus be larger than the RC recovery time at the collector of a transistor. This gives a speed penalty for such a cell which can be written as

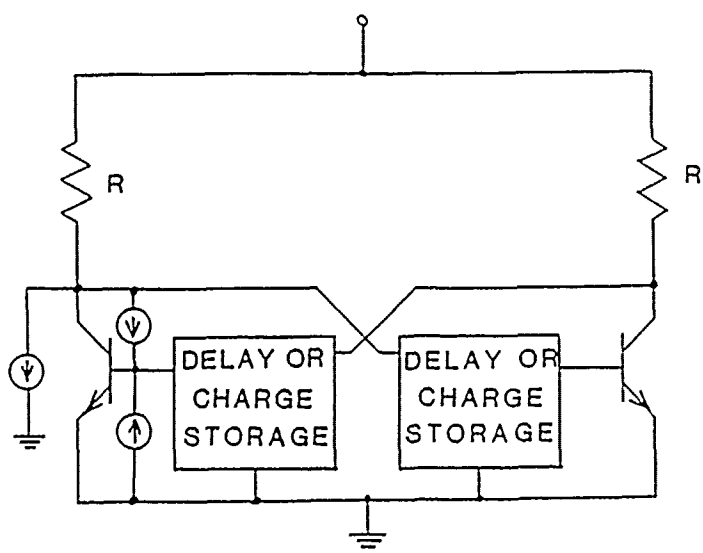


Figure 56. Illustration of hardening approaches using various types of feedback-delay of charge-storage elements.

$$T_d > R_L C_{TC} , \qquad (8)$$

where C_{TC} is the total collector node capacitance. Using the previous capacitance values (C_{CI}=0.1pF) and an R_L=40kΩ (0.1m Watt/cell at 2V) gives T_d > 4nsec. This gives an estimate of the speed penalty which any feedback scheme must suffer. In some applications such a penalty may be acceptable.

A more important problem with any such bipolar feedback scheme concerns a device hit on the emitter and/or the base. Such a hit gives current sources directly into the base in Figure 56. Thus for such hits, feedback is no longer needed to increase the base voltage as well as decrease the collector voltage. The hit transistor can thus go to a low-impedance state without the action of the feedback and both transistors end up in a low state. For such a situation, both transistors in Figure 56 lose the information with regard to the initial state of the RAM cell. If the cell is to recover from such a base-to-collector current pulse, information regarding the previous state of the cell must be retained within the feedback path itself and used to recover the original state of the cell. Another critical factor in a hardening approach appears to be the ability to isolate the charge storage mechanism in the feedback path from the perturbations on the hit transistor. For example, if the charge storage element in the feedback path can discharge to the low collector node of the hit transistor then it can not be effective in restoring the previous state of the cell. Similarly, if the storage element can be charged by the positive base voltage on the hit transistor, the previous state can not be recovered.

A feedback technique satisfying these general requirements has been proposed by Messenger, et al. [150]. This approach uses one or more emitter followers in the feedback path between the collector and the base. Charge stored in the emitter follower provides the required stored charge to keep the initially "on" transistor in its conducting state while the hit transistor recovers from the single event current pulse. P-n junctions in the emitter followers also provide isolation of the hit transistor from the base feedback path while the transistor recovers. The emitter followers provide a time delay between the hit event and the loss of charge to the normally "on" transistor and during this time the hit transistor can recover and the cell can return to its initial state. In a specific design example, Messenger, et al. [150] have compared cells with 1, 2 and 3 stages of emitter followers and predicted by computer simulations improvements in critical charge by factors up to greater than 10^4 for 3 emitter followers, with increases in low-to-high transition times of 18 nsec.

Another approach to SEU hardening at the cell level is to use some type of local redundancy. Belt, et al. have proposed one such approach [151] which duplicates the basic RAM cell such as shown in Figure 48. The duplicated cells have a common base connection but the collector feedback paths are arranged in a hard wired OR arrangement so that two collectors must go low in order to switch the memory state of the cell. An SEU event which pulls one collector low will not upset the cell regardless of the deposited charge. The OR gated feedback eliminates collector-substrate charge collection from causing upsets but does not completely harden the cell

since base-collector or base-emitter currents directly turn on both transistors. This technique, however, can significantly improve the overall error rate by eliminating the large collector-substrate sensitive area. The use of feedback delay is also discussed by Belt, et al. [151].

Once one accepts the basic need for local redundancy and additional storage nodes, RAM cell configurations other than that of Figure 56 are possible. Figure 57 shows a four invertor storage cell in a loop configuration. This has two high nodes alternating with two low nodes. Input and output can be from any adjacent pair of cells. Information regarding the memory state of the cell is retained regardless of which transistor in the cell is hit by a high energy particle.

SPICE simulation of SEU hardness of several cell configurations have been performed. The device parameters in Table 11 have been used as typical of a 2 μm Schottky clamped bipolar technology. To simplify the calculations, a single current pulse into the base has been used. As far as circuit operation is concerned, this has very little difference from a collector-to-base current pulse when the collector is driven to a low voltage.

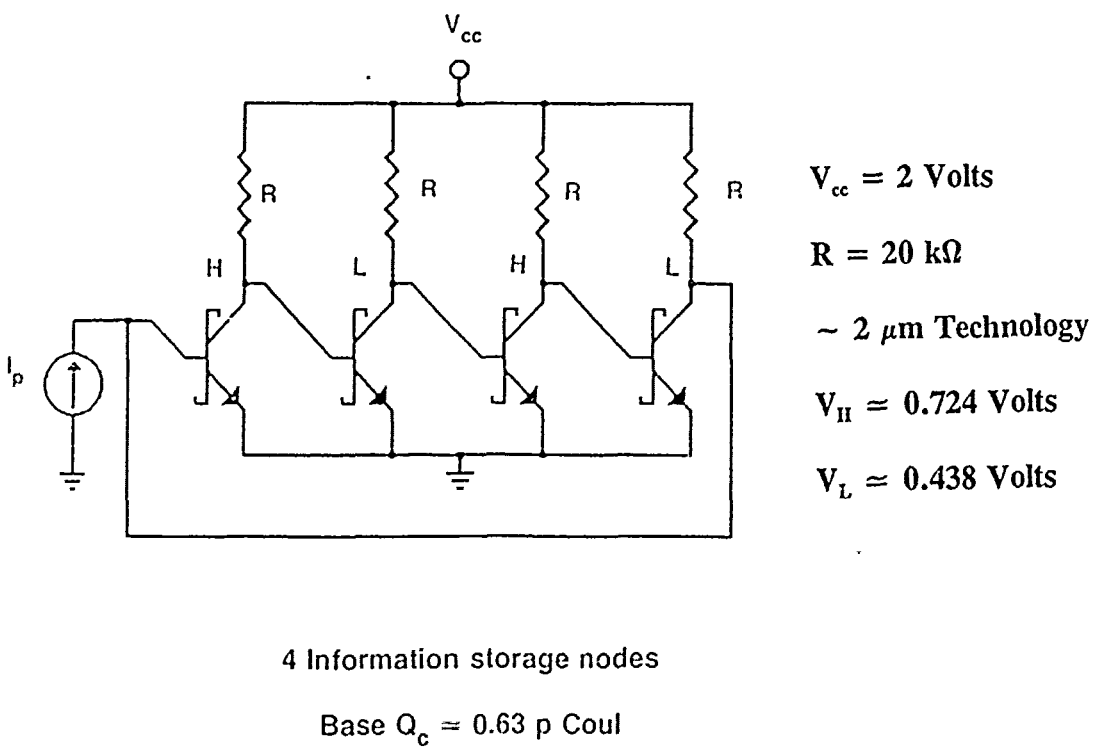
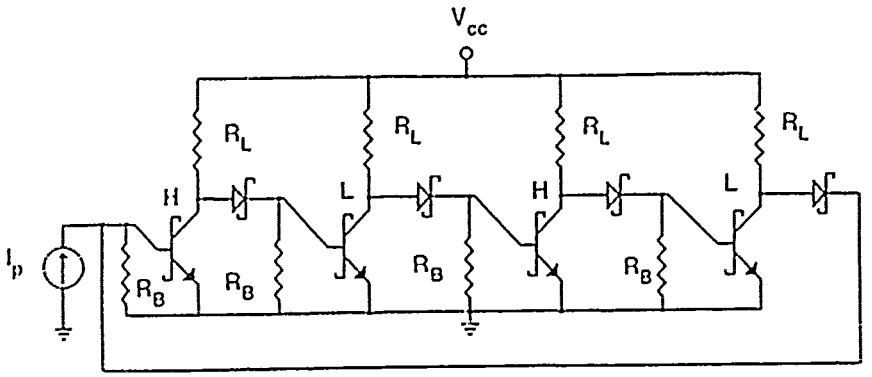


Figure 57. Four inverter Schottky RAM cell.

The four invertor configuration of Figure 57 shows some improvement in SEU hardness over simple two invertor cross-coupled cells because of the additional delay in the feedback path. SPICE simulations have given a critical change of 0.63 pCoul for Figure 57 as opposed to 0.18 pCoul for a single RAM cell. This factor of 3 improvement is however not very large. A modification of Figure 57 as seen in Figure 58 does however produce an SEU-hardened cell design. This design further isolates the information storage nodes with additional Schottky diodes and results in eight independent nodes. The critical charge of the cell is controlled by the resistors R_B and was found to go from 5.5 pCoul at R_B = 100 Ω to 2,500 pCoul at R_B = 200 kΩ.

The physical mechanism by which the cell is hardened can be readily understood with reference to Figure 59. The Schottky diodes serve to effectively isolate the hit transistor from the remainder of the circuit immediately following a change of state of the hit transistor. The Schottky diode at the collector of the leftmost transistor in Figure 59 become reverse biased as the base rapidly goes high and the collector rapidly goes low. Without the high transistor drive of the leftmost transistor, the base voltage of the first low collector transistor begins to decrease with an RC time constant determined by R_B and the transistor device capacitances shown dotted in the figure. The first low transistor will eventually go high followed by switching the next high transistor low, etc. There are two basic RC time constants preventing the latching of the



V_{cc} = 2 Volts

R_L = 20 kΩ

~ 2 μm Technology

$V_H \simeq$ 0.999 Volts

$V_L \simeq$ 0.444 Volts

8 Independent nodes

Base $Q_c \simeq$ 5.5 p Coul for R_B = 100 kΩ

Base $Q_c >$ 2,500 p Coul for R_B = 200 kΩ

Figure 58. Hardened Schottky-based RAM cells.

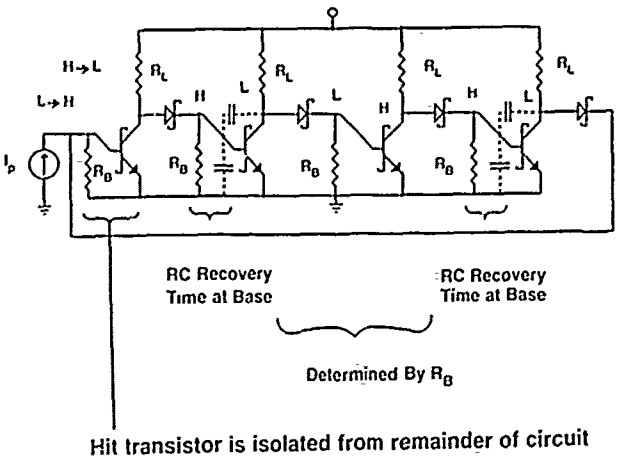
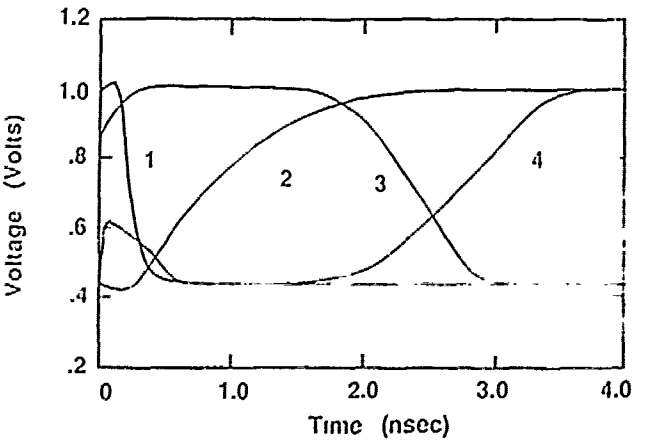


Figure 59. Illustration of hardening mechanism for Schottky based RAM cell.

hit transistor state permanently into the cell. The hit transistor recovers with its own internal time constants which are also influenced by R_B . The recover times are determined to a large extent by R_B and thus critical change can be adjusted by changing R_B.



Time Delay in Inverter String Outputs

(R_B = 100 kΩ)

Figure 60. Voltage delay waveforms for hardened Schottky RAM cell.

The time delays in a four invertor string are shown in Figure 60 for R_B=100kΩ, when the base of the first stage is rapidly driven high. As can be seen there is about a 3 nsec delay through the four stages during which time a hit transistor has time to recover.

SEU hardening is achieved at some expense to write time in all circuit level approaches. This has been briefly studied for the four invertor hardened cell of Figure 58. In any circuit, write time depends on the current drive from the access transistors which are not shown in Figure 58. The two invertor cells was found to have a write time of 1 nsec with a write current of 0.6 mA. The four invertor cell required 1.0 mA for a write time of 2 nsec. This is not a sever time penalty but would require a larger drive current source.

By using two locally redundant RAM cells connected in a hard wired OR configuration, it is possible to obtain an unconditionally SEU hard cell. This is shown in Figure 61. The layout is basically that of two invertor cells with the collectors wired in a OR configuration to supply base drive to the opposite sides of the RAM cell. The OR configuration is based upon the fact that a high energy particle can cause a high collector to go low but can never cause a low collector to go high. The collector of any high transistor can be taken low for any desired period of time and the other redundant high side will retain the logic state information and the cell will recover.

The Schottky diodes at the bases of the transistors are required to make the cell hard for a collector-base current source. In such a case, the Schottky diodes at the collector and base essentially isolate the hit transistor from the remainder of the circuit allowing it to recover at any internal time rate. This cell is thus unconditionally SEU hard for any combinations of current sources as long as only one of the high transistors is influenced by a high energy particle. Careful circuit layout will be required to insure no multiple device hits by a single particle. Computer simulations have verified that this ORed-collector SRAM cell is unconditionally SEU hard.

6.7 SUMMARY AND CONCLUSIONS.

In this section a review has been presented of SEU effects in bipolar RAM cells. This has ranged from the basic charge collection process in transistors, to circuit level effects and modeling. The basic SEU effects in bipolar RAMs are characterized by a few relatively simple concepts and can be approximated by relatively simple models. It is emphasized in this work that the fundamental concepts limiting critical charge and RAM cell upset rates are similar for all logic types. New approaches have recently been proposed and simulated by computer analysis which offer promise of significantly increased SEU hardness for bipolar RAMs. These are circuit level techniques of somewhat greater complexity than resistor decoupling in CMOS cells. The area and power penalties of these hardening approaches are more severe than for CMOS resistive hardening. Further work will likely lead to improved hardening techniques beyond those presently known.

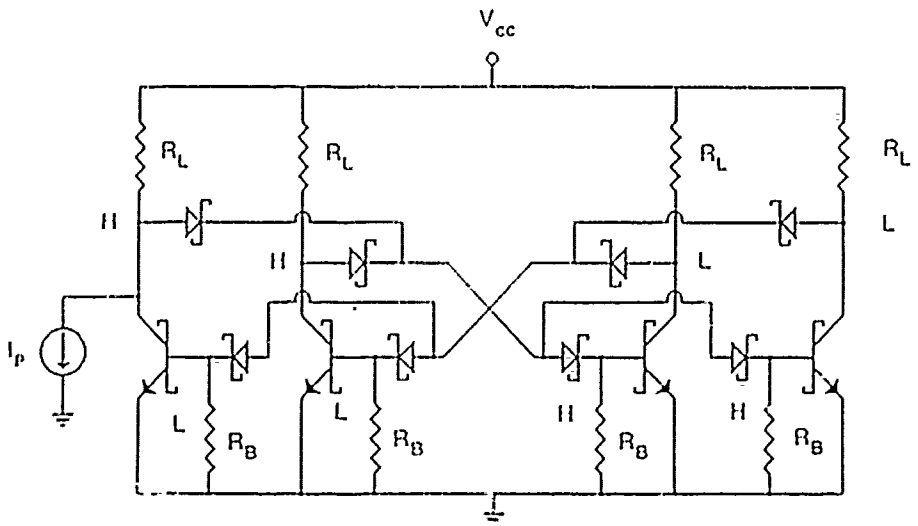


Figure 61. Unconditionally hard RAM cell using local redundancy and Schottky diode isolation.

SECTION 7

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APPENDIX A

THE USER MANUAL FOR PARA

This section describes all the necessary commands and the files that the user needs to know about before using PARA. Various input and output options and the file formats are presented.

A.1 GETTING STARTED.

PARA can be executed by using one of the following command forms.

```
para intInterval circuitFile
para circuitFile
```

In the above two cases, the circuitFile refers to the circuit description file. The description is essentially the same as the SPICE description with some modifications and will be discussed in the following section. The intInterval provides the interpolation interval to be chosen for the doses that are present in a file containing transistor parameters at various dose levels. The use of this interval is described in the following sections.

PARA reports all output information on its standard output. In case the output needs to be filed, it can be redirected into the desired output file. The above commands in such cases can be modified to the following:

```
para intInterval circuitFile > outputFile
para circuitFile > outputFile
```

A.2 INPUT FILES.

PARA needs several kinds of input files. These files contain information about the circuit and the parameter shifts of its devices due to radiation. The various files required by PARA are the following:

Circuit description file
.model file
.res file
-int.res file
inverter file

The various files are described below.

A.2.1. Circuit Description File.

This file contains details of the circuit which PARA is supposed to test. The input file format is the same as the SPICE format with a few additions.

Transistor Declaration. As in SPICE, transistors are represented by a string starting with the letter 'm' or 'M'. The rest of the word is immaterial and is ignored by PARA. The string can be used by the user to distinguish between the various transistors. A general form of the transistor declaration is shown below.

> MpullUp drain gate source substrate modelName [w = 10u] [l = 2u] [as = 10e-15] [ad = 10e-15]

where "drain" is the node name of the drain of the transistor, MpullUp. "source" is the node name of the source of the transistor, MpullUp. "gate" is the node name of the gate of the transistor, MpullUp. "substrate" is the node name of the substrate of the transistor, MpullUp.

All of the above PARA node names are strings; SPICE nodes are designated by numerical numbers. The names "VDD" and "vdd" are reserved for the supply voltage. Similarly, "GND" and "gnd" are reserved for the ground. All reserved words can be used either in uppercase or lowercase, but not in a combination of upper and lower cases, i.e. vDD, Vdd, GnD etc., are not allowed. In addition, the names should not exceed 10 characters.

"modelName" refers to the name of the model associated with the transistor, MpullUp. The model itself can be defined anywhere in the circuit file. Figure 62 provides an example of the model definition. All the other variables existing in the declaration are optional. Default values are used if any variables are left unspecified. The above optional parameters, with their meanings and default values are shown in Table 12.

An example of the transistor declaration is shown below.

```
MpassTran  output input vdd vdd cmosp w=10u l=2u
```

A maximum of two lines for the transistor declaration is allowed. The second line should begin with a '+' in the first column in order to represent continuation from the first line. The above example if extended to two lines would look like the following.

```
MpassTran  output input vdd vdd cmosp w=10u
+ l=2u
```

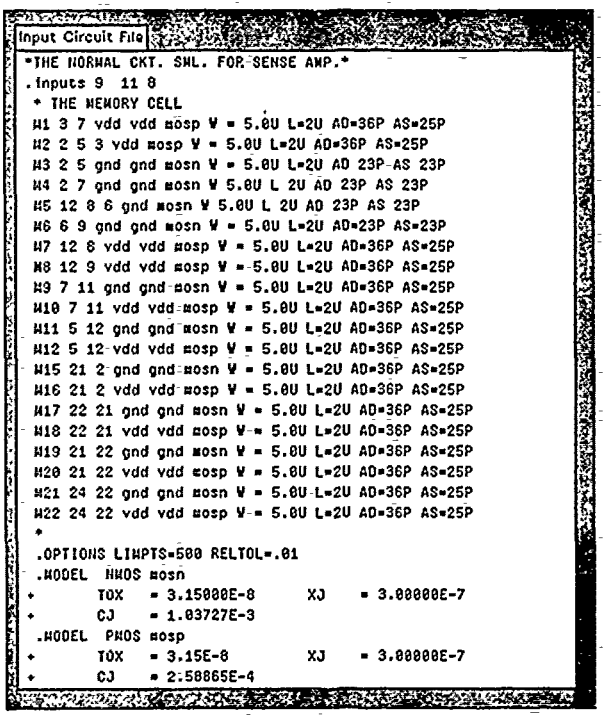

Figure 62. An example of Model definition.

Table 12. Default values for model parameters.

Parameter Symbol	Parameter Meaning	Default Value
TOX	Oxide thickness	520E-10 m
CGSO	Gate to source overlap capacitance	5.2E-10 f
CGDO	Gate to drain overlap capacitance	5.2E-10 f
CJ	Junction capacitance	4.5E-4 f
RON	On resistance of the device when it was ON during irradiation	1000 ohms
ROFF	On resistance of the device when it was OFF during irradiation	1000 ohms
RONLEAK	Off leakage resistance of the device when it was ON during irradiation : n-devices only	10000 ohms
ROFFLEAK	Off leakage resistance of the device when it was OFF during irradiation : n-devices only	10000 ohms

Resistor and Capacitor Declarations: A typical resistor declaration starts with an 'r' or 'R' and has the following form:

RpullUp vdd output 10K

This represents a resistor between "vdd" and "output" nodes with value 10 kiloohms. A capacitor has a similar form except that it starts with a 'c' or 'C'.

.inputs CARD.

.inputs CARD specifies all the inputs of the circuit. PARA performs the delay calculations only through the paths containing these inputs. Therefore, the user has the flexibility of specifying a part of the circuit for delay calculations. A typical input declaration looks like the following:

.inputs inp1 clock control1

Here inp1, clock and control1 are the input nodes to be considered.

.model CARD.

.models CARD specifies the model to be used with the transistors declared above. The modelNames associated with transistors are defined in the .model CARD. An example is seen in Figure 62.

.mod File.

.mod file contains the SPICE model parameters at each dose level along with other parameters desired for failure calculation. PARA uses this file, along with SPICE and an inverter chain file (described later) to calculate the equivalent ON and OFF resistance values at each dose level. This file should exist in a subdirectory PARAfiles and there has to be one .mod file for all fabrication processes. For example, if the given circuit is to be analyzed using the Sandia fabrication process, a file PARAfiles/Sandia.mod should be present. The format for the file is shown in Figure 63. The first line contains the keyword '.dose' and the corresponding dose value. The second line contains the keyword '.leakage' and the OFF resistances of the n-channel transistors under the condition when they were ON and OFF during radiation respectively. These resistances effectively represent the leakage through the transistors when the node voltage is going HIGH. An example of .leakage line is given below.

.leakage 1.0e8 1.0e9

This means that the OFF resistance of the n-channel transistors is 1.0e8, if it was ON during

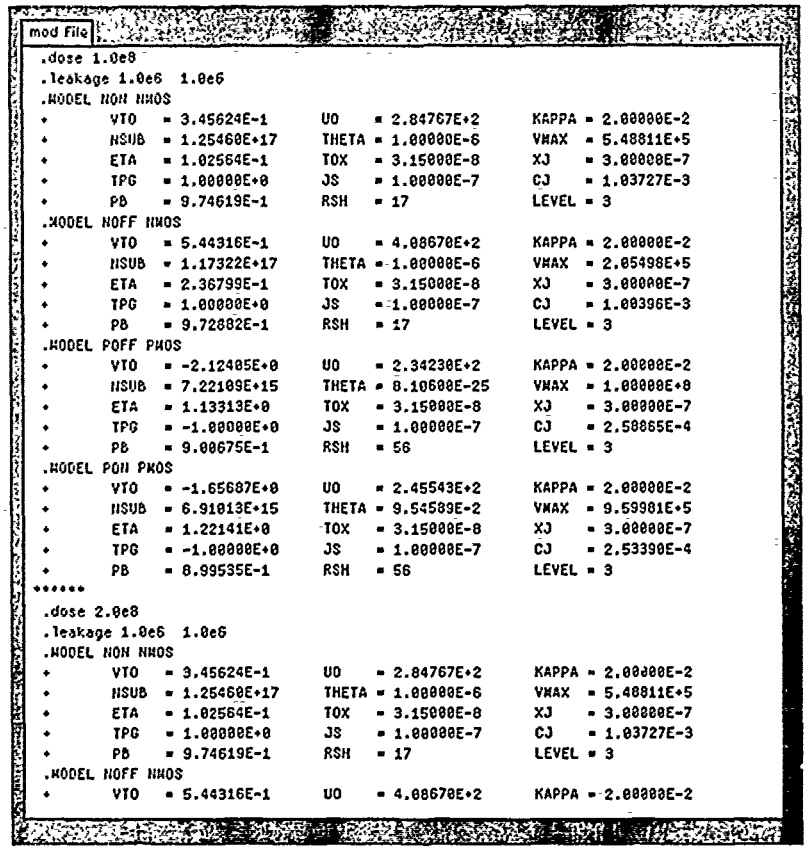

Figure 63. Format for .mod files.

irradiation, and 2.0e9 if it was OFF during irradiation.

The next few lines describe the SPICE model parameters for all the desired conditions i.e. p-channel transistor parameters if it was ON during radiation and OFF during radiation. The same holds for the n-channel transistors. The last line should necessarily begin with an asterisk to mark the end of the dose parameters. After every dose level, a line with the asterisk is essential.

.res File.

This file, present in the subdirectory PARAfiles, is created by PARA only if it is not already present. PARA uses the information in the .mod file and runs SPICE on the inverter chain (inverter file is described later) and extracts the resi .ance values. The ON resistances of n- and p-channel transistors for the particular fabrication process are generated and placed in this file. An example of this file is seen in the Figure 64. The initial two lines are the same as in the .mod file but the next line contains 'non' 'noff' 'pon' 'poff' . 'non' and 'noff' mean n-channel ON resistance if it was ON during irradiation and n-channel ON resistance if it was OFF during irradiation, respectively. 'pon' and 'poff' have similar meanings. The last line, which represents the end of all the parameters for the particular dose level starts with an asterisk.

```
.dose 1.0e8
.leakage on 1.0e10 off 1.0e10
pon 275000.031250 poff 199999.968750 non 174999.796875 noff 124999.968750
******
.dose 5.0e8
.leakage on 0.5e10 off 0.5e10
pon 375000.031250 poff 299999.968750 non 124999.796875 noff 104999.968750
******
.dose 10.0e8
.leakage on 0.25e10 off 0.25e10
pon 475000.031250 poff 399999.968750 non 74999.796875 noff 64999.968750
******
```

Figure 64. Format for .res files.

This file can either be created by PARA or by the user simply by editing the file in the appropriate format. Once the file is present in PARAfiles, PARA does not recreate it for other circuits. The same parameters are valid for all the circuits which are to be fabricated by the same technology. For Sandia.mod, the .res file should be Sandia.res.

-int.res File.

In case the user provides the option of interpolation with a specified interpolation interval, PARA creates -int.res file from .res file using linear interpolation. In case the interpolation option is given by the user, PARA creates this file even if it is present in the subdirectory PARAfiles, since the interpolation interval may be different. If the .res file present is Sandia.res, the corresponding file generated is Sandia-int.res. The file can alternatively be generated by the user simply by editing the file using the same format as the .res file.

inverter File.

This file is needed at the initial point when .res file is to be generated from the .mod file. This file is to be present and should always be named as invchain. PARA runs SPICE on the inverter

file to generate the various resistances using different models in the .mod file. This essentially means that the first run on a circuit with a new technology, PARA is going to be slow, since SPICE is to run for all the sets of model parameters in the .mod file. All other runs, on different circuits but using the same technology (fabrication process) will take less time. The inverter file is always the same and is shown in Figure 65. Also at the beginning, the user should make sure that SPICE is runnable from the directory where PARA resides, i.e. an executable version of SPICE is to be present in the directory or an appropriate path should be set.

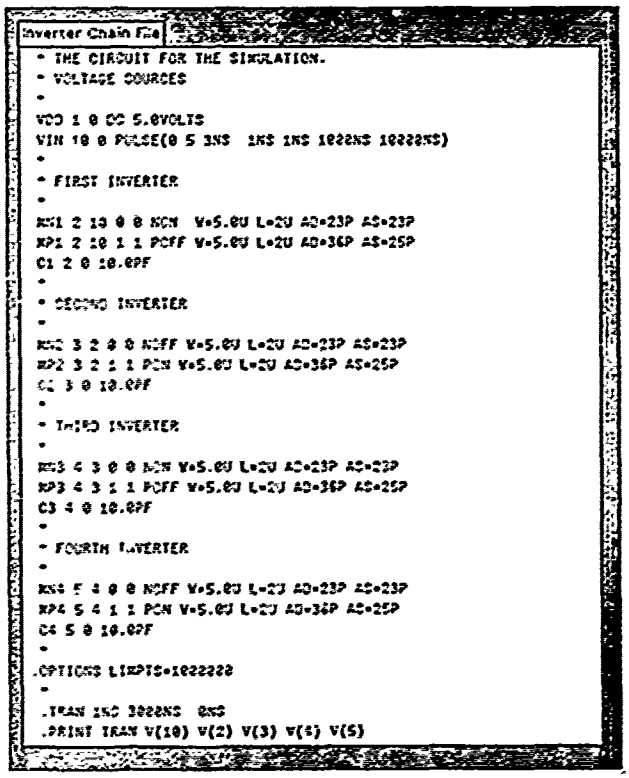

Figure 65. Inverter file for resistance extraction.

Output Files.

PARA does not generate an output file directly. All the output information is printed on the standard output. In order to file the output, redirection of the output to a file can be requested. PARA then prints out the node degradations, path degradations, power-supply degradation for each dose level. The percentage variation from the zero dose level is specified and it is left to the user to determine if the degradations are large enough for the failure to occur.

Input Options.

Several options are available based on the kind of data files that are available. During the first run on a circuit using a particular technology, the .res file is normally not present. The user

therefore has the flexibility of either providing the .mod file which can be used by PARA to generate the .res file or the user can edit the file manually filling all the data required in the .res file. PARA essentially checks if the .res file exists in the PARAfiles directory. If it file is present, then PARA uses it directly, else PARA first tries to generate the file using SPICE, .mod file, and the inverter file, and then uses it on the input circuit. For all the subsequent runs on different circuits, but using the same technology (e.g.Sandia), it uses the .res file generated.

In case the -int.res file is present in the directory PARAfiles, this file is given preference over .res file i.e. -int.res file is used rather than .res file. The user has the flexibility of providing the interpolation intervals as desired. Whenever the interpolation intervals are provided in the command line, PARA uses the interpolation on .res file to generate -int.res file regardless of whether -int.res file is already present in PARAfiles. Therefore if the user wants to preserve a number of -int.res files with different interpolation intervals, he or she needs to rename the files to different file names before providing the new interpolation interval to PARA. In case the -int.res file is absent and no interpolation option is given in the command line, .res file would be used. As with the other files, the user can edit the -int.res file himself keeping in mind the appropriate format. By using the interpolation options and the combination of various files, a number of input options are possible.

Limitations.

There are some restrictions on the kind of circuits that the current version of PARA can handle. Only CMOS Digital circuits can currently be analyzed. These include all the gates, latches and pass transistors (transmission gates). The circuits that are out of PARA domain are the ones that do not have equal number of complementary p- and n-channel transistors. Any form of analog circuitry which may occur in digital circuits, including sense amplifiers and dynamic RAMs, are not handled. External resistances are not handled in the current version. In addition, the capacitances at nodes other than signal nodes are ignored.

PARA provides accurate delay values for most cases. For cases when a very slow element is present in series with a sequence of fast elements, PARA does not provide very accurate delay values, but correctly identifies the critical path. As in any other switch-level simulator, PARA sums up the delays at individual gate nodes to obtain the total value. In actuality, two consecutive gates have an overlap of real time during which they approach their final value. Therefore, the addition of delays to get the total delay is not precise. The error introduced by this summation is very small for most cases, except for the circuit paths having extremely slow elements. Such paths are therefore, not handled properly by PARA. PARA provides higher delay values in such cases and hence is pessimistic in nature. This situation can be seen more clearly, if we assume that the external capacitance at a node in a circuit being simulated has a value 10 uF instead of 10 pF. In this case, that node rises to a HIGH level (5 volts, say) very slowly as compared to other nodes. As it rises to 2.5 volts, it starts affecting the next gate and therefore the output of that gate starts falling to LOW level simultaneously. The possibility of this output node reaching the LOW level before original reaches the HIGH level cannot be ruled out. This clearly indicates

that the total delay in this case cannot be the sum of the delays at these nodes. PARA does add up the delays and provide a higher value of total delay.

PARA carries out a linear interpolation of the parameters for the intermediate dose values. This is not very accurate if the data points available are far apart. Accurate results are expected if the parameters in .res file are available at small dose intervals.

PARA does not simulate failures due to field-oxide leakage.

A.3 SOURCE CODE FILES.

Important source code files are briefly described here.

Main file.

The main file that controls the sequence of operations and contains the main function is para.c.

Include files.

These files are included into most of the other source code files. They contain all the data declarations and constant definitions.

i. constant.i

This file defines all the constants used in all .c files.

ii. struc.i

All the structures for devices, capacitances, signal nodes and signal paths are defined here.

iii. def_str1.i & def_str2.i

These define some of the default values for device parameters and are easily changeable.

Input Interface Files.

These files control the front end and interact with SPICE for the extraction of relevant parameters.

i. resistors.c

The ON resistance values of the devices are calculated by this file.

ii. modifyres.c

This function in this file changes the resistances of the devices after each run for a dose.

iii. interpol.c

Interpolation of the resistance values is carried out by the function defined in this file.

Database Generator Files.

These files parse the input circuit description file and generate the database for subsequent failure simulations.

i. getdevice.c

All the resistor and capacitor declarations are scanned and placed into appropriate data structure.

ii. getr.c

The transistor declarations are read and stored.

iii. putmodel.c

The models corresponding to the transistors stored are attached to the transistor descriptions.

iv. inputs.c

.inputs card is read and the input nodes are stored for subsequent signal flow generation.

v. getnode.c

All the signal nodes are extracted and the transistors associated with them are stored along with them.

vi. sig_cap.c

The node capacitances are calculated and attached to the description of the corresponding node.

vii. sigflow.c

The signal paths are generated for dynamic failure calculations.

Failure Detection Files.

The failure simulation algorithms are implemented in these files.

i. minpath.c

The n-channel and p-channel resistances for static failure determination are calculated in this file. Power supply related failure is also handled in this file.

ii. delay.c

Dynamic failure calculations are done by the functions defined in this file. The individual delays at each nodes are calculated and added to form the total delay.

Other Files.

These files do not fall into any special category.

i. loads.c

This file loads a single line from a file into a buffer.

ii. getword.c

This file allows a word to be loaded into a buffer from a line stored in another buffer.

ii. makefile

This file generates PARA for execution.

APPENDIX B

AUTOMATED IMPLEMENTATION AND EVALUATION OF CIRCUITS

B.1 INTRODUCTION.

It has been shown in the past that there are three distinct failure modes for a CMOS IC when exposed to radiation [16]. They are (a) power-related failures, where increase in leakage currents increases standby power too high for proper operation, (b) static failure, where increased n-channel leakage combined with decreased p-channel drive produces nodes in indeterminate logic state, (c) dynamic failure, where delays along a signal path are too large for synchronous operation. The mechanism involved in the above failure modes is the changes in device parameters including threshold voltages, carrier mobilities and leakage currents. In general the threshold voltages of n-channel devices decrease and those of p-channel devices increase (negatively) with increasing total-dose radiation[6, 17]. The carrier mobilities of the devices decrease and the n-channel leakage increases. Besides parameter shifts, another failure mechanism, FOX failure, exists where the region under the field oxide forms a channel to make a parasitic depletion mode device. Most design oriented hardening techniques involve changes in the layout parameters such as widths and lengths of transistors. Table 1 shows various failure modes under total-dose irradiation, their mechanisms and the corresponding hardening techniques used. Testing and hardening ICs against dynamic failure has been the focus of study in this project.

Figure 66 shows the design-level factors that can affect the radiation tolerance of circuits. The radiation tolerance of a digital circuit is contingent on the magnitude of the degradation of circuit parameters e.g., maximum delay, power requirements and voltage levels. The degradation of circuit parameters is a direct consequence of the shifts in device parameters caused by total-dose radiation as explained above. It has been seen that the magnitude of device parameter shifts depends not only of the total dose and dose rate of radiations but also on the bias of the devices during irradiation[8]. This is due to the bias dependency of the charge trapping on each of the failure mechanisms. Input vector to the circuit is one of the factors that determine the bias for the devices inside the circuit. For an n input digital circuit, 2^n input vectors are possible. Consequently, 2^n number of possible bias conditions exist. The same circuit can therefore degrade in 2^n possible ways for the same dose. Another factor that affects the internal bias is the design implementation i.e., the choice of gates. Two different implementations of the same logic can result in a different number of gates, transistors and the nodes in the circuit. The node voltages and hence the bias during irradiation will be different. The information about the input vector and the particular implementation of the design of a circuit is, therefore, of utmost importance for testing the radiation tolerance of the circuit. Experimental results have been obtained proving the above mentioned bias dependency on failure-exposure level for different implementations of the same function.

Table 13. Failure modes, mechanisms, and hardening approaches.

IC Failure Mode	Failure Mechanism	Hardening Techniques	
		Process	Design
Power failure	FOX Leakage	Channel stop, Trench	Layout width
	Edge Leakage	Rad Hard Technology	Gate oxide extension
Static failure	Same as dynamic	Rad Hard Technology	Layout
Dynamic failure	Vth (Nit & Not)	Rad Hard Technology	
	gm (Nit)		
	FOX leakage		
	Edge leakage		

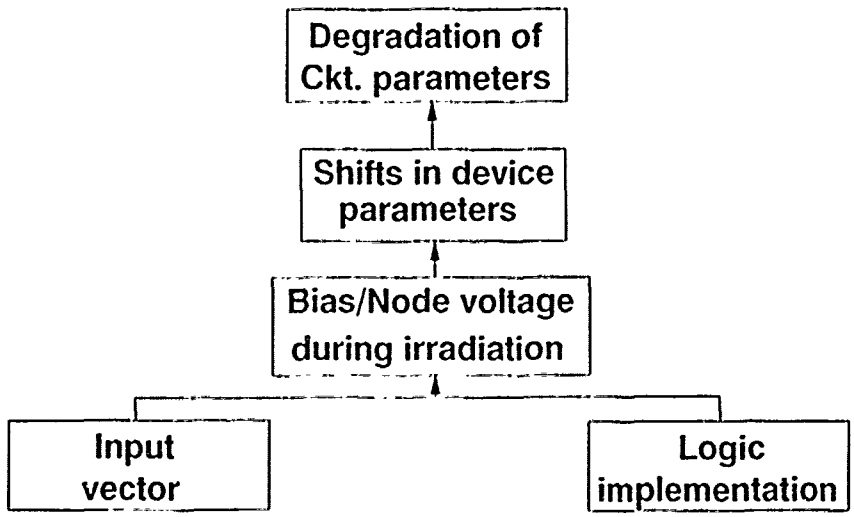

Figure 66. Design-level factors affecting radiation tolerance.

B.2 HARDENING AT LOGIC LEVEL.

The above discussion also points towards a new methodology to harden ICs against radiation. As each of the different design implementations of a function has different radiation tolerance, an optimum logic-level design can be identified for increased radiation hardness. The conventional method for hardening an IC has been to change the fabrication process parameters to achieve

required hardness. However, now we have reached a stage where increases in radiation tolerances through improved fabrication processes are not worth the cost. The submicron fabrication processes require extremely high manpower and expenses to accommodate any changes. The increases in radiation tolerances through improved device-level designs are an attractive alternative [16]. However, increases achieved through this methodology have limitations due to the increased silicon space requirements. To design a given boolean function using optimum combination of logic gates may be another alternative. In fact, maximum hardness for an IC can be achieved through the combination of these three approaches. The first two approaches have been well documented in the literature. In this paper, we will describe the third approach of identification of best logic-level design for any given boolean equation based on our experiment.

The device parameter shifts for devices similar to Sandia devices will indicate that the NAND gates are inherently harder than NOR gates. However, this applies only for static failure mechanism where the parallel configuration of n-channel devices and series configuration of p-channel devices cause minimum current available for charging up of an output node. However, this can be avoided by using properly ratioed device widths and lengths. The above misconception of superiority of NAND gates has caused designers to use only NAND gates in their designs. This again increases silicon space requirement, design time, and may not yield the best possible design.

B.3 SOFTWARE AUTOMATION FOR RADIATION-TOLERANT DESIGN.

The best possible design for a given boolean logic function can only be achieved through exhaustive search in the design space. Due to endless possible ways to design a circuit, this approach is not worth the computational price. New heuristic methods must be developed to identify the best possible design in terms of area, speed, and radiation tolerance. We have developed such a design tool which takes a boolean expression as an input and presents to the circuit designer, possible circuit designs along with parameters like area, speed, power requirements and radiation tolerance estimates. The number of possible implementations are greatly reduced by using the branch and bound technique of removing tree branches with cost more than some specified value. The costs are in terms of the above parameters and can be adjusted externally by the designers. Although the worst case time complexity of this algorithm can be exponential, the expected time complexity is greatly reduced to a polynomial. The reduction of the boolean expressions are achieved by using Quine-McClusky algorithm[18-20], a systematic reduction algorithm permitting routine processing of digital functions. This algorithm essentially involves tabular minimization of functions with large number of variables. The method, conceptually, is similar to the traditional Karnaugh map method, but is more suitable for programming.

The algorithms use the knowledge that there are only four different failure mechanisms possible for a circuit. Out of these, FOX failure and static failures are not considered due to the fact that they can easily be corrected by the circuit designer through conservative layout design rules and device level designs. For the dynamic failures, our algorithm first creates a circuit with shortest

possible signal paths in the design. Based on this design, DeMorgan's theorem is used to modify and obtain designs with least number of gates. All other designs with path length close to the optimum one is also preserved for inspection by the circuit designer.

The software takes as input a boolean function and creates various possible circuits and analyzes them on the basis of area, power, maximum delay and radiation degradation. The allowed gates, along with their parameters including input and output capacitance, pull up and pull down resistances and the changes of resistances with radiation are provided by the user. The user is permitted to compare the values of the circuit parameters for all the designs in order to choose a design best suited for him. In most cases trade offs are necessary since a circuit with best radiation tolerance may take up larger area or consume too much power.

A 2-bit magnitude comparator designed by this software provided the results shown in Figure 67. Four designs were output by the software along with their comparative performance. In the figure, circuit marked by the digit 1 appears to have the best performance with respect to delays before and after irradiation and the area. Nevertheless, this circuit takes up more area than the circuit labeled with digit 3. Circuit 3 on the other hand is least tolerant to radiations as seen in the figure. Similarly circuit 2 has less delay than circuit 4, but occupies more area. Such data can be significant in choosing an appropriate design for a particular application. Larger circuits can also be implemented and the circuits obtained can provide substantial help to a user designing radiation hard circuits.

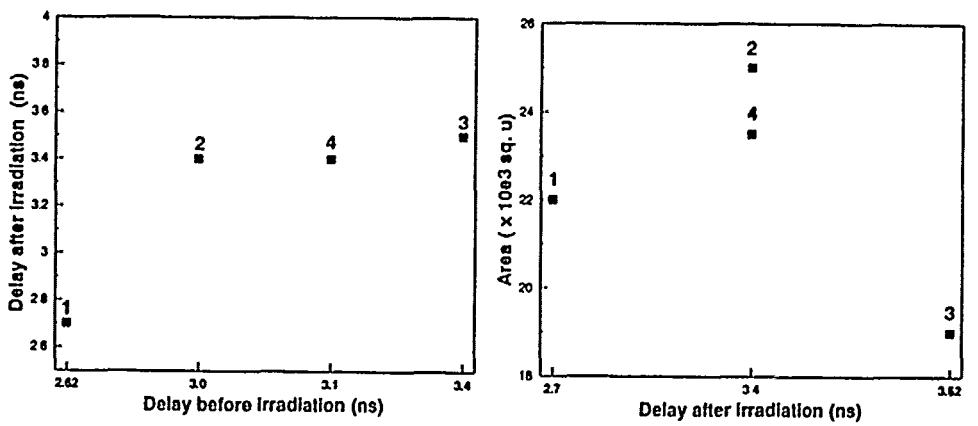

Figure 67. Results for a 2-bit magnitude comparator from AIEC.

The availability of such a design tool along with PARA, a device-level tool, will give the circuit designers power to combine all the three hardening methodologies to achieve the maximum radiation tolerance through current technology. This design tool provides various implementations

of a circuit to the user whereas PARA extracts the worst case bias conditions for each of these implementations. Together, these tools can be very effective in designing and testing radiation hard integrated circuits.

B.4 CONCLUSIONS.

It has been shown by simulations and experimentally verified that the logic implementation of a circuit and the bias applied during irradiation are significant in determining the radiation tolerance of ICs. A software package has been introduced that uses these facts to aid a designer in designing radiation hard integrated circuits.

APPENDIX C

PARASTAT

C.1 INTRODUCTION.

The requirement for increased functionality per chip has forced increases in device densities and decreases of minimum feature size on an integrated circuit (IC). This scaling of feature size has progressed more rapidly than the scaling of process tolerance. Still, process tolerance has led designers to incorporate the assumption of low parameter spreads into their designs. Advanced circuits are more sensitive to a particular parameter spread than are older designs. As a consequence, the statistical variations of device characteristics on an IC can be not only significant determinants of yield, but also of performance relative to the simulated, "ideal" performance. In addition, statistical variations can affect the reliability of the ICs in the field, especially in radiation environments where these variations are amplified by the independent statistical variations due to bias-dependent individual device parameter shifts [21]. The methodology currently in practice determines the radiation tolerance of a lot (fabrication process) based on the results of radiation exposures on samples. Average parameter shift values, rather than statistical distributions are used to characterize the process. The fundamental assumption on which this technique is based is that a small sample from a given process can be used to accurately represent all other devices from that process. This assumption will not be satisfied if there is significant lot-to-lot variation in parameter values or distributions. Simulations modeling the affect of statistical variations during fabrication and those introduced by irradiation can provide useful support to lot tests by assessing the validity of their fundamental assumption.

One such technique, proposed by Rogers et al. [22] is to use the test devices and special circuit simulators to access the radiation tolerance of parts. For their approach, each IC is designed to contain arrays of transistors in the kerf area. During testing, only this area is exposed to radiation and the characteristics of the individual transistors in the array are recorded. The transistor parameters from kerf area are expected to vary statistically, or vary within a given range. With the help of special circuit simulators, the information obtained from testing of individual transistors can be used to estimate the radiation tolerance of the individual IC. The basic assumption here is that the transistors in the kerf area will have behavior representative of the transistors on the IC. Due to close proximity of these transistors to the real circuits, this is a very reasonable assumption and should yield accurate reliability analysis.

For the above mentioned approach to yield accurate results, the transistor-level characteristics must be transformed into a chip-level performance degradation analysis. It is well known that the bias-dependent device parameter shifts for individual devices make the conventional circuit simulation of radiation effects a very difficult process, even when reliability and statistical are not taken into consideration. PARA, employing switch-level algorithms and simple RC-delay estimation techniques has been developed for conventional simulation and failure analysis of

total-dose radiation effects on CMOS ICs. However, the algorithms employed in PARA accept only precisely defined transistor parameters for p- and n-channel devices. We have modified this simulator to accept statistically varying device parameters or ranges of device parameters, thereby adding a reliability analysis capability. This modified simulator is called PARASTAT.

C.2 SIMULATION OF STATISTICAL PARAMETER VARIATIONS.

The main purpose for the development of PARASTAT is to incorporate data from testing of device arrays in kerf area into efficient simulations of circuit radiation tolerance and reliability. The set of device parameters obtained from individual tests will be represented in PARASTAT either as a value range for each parameter or as the statistical description of the parameters, assuming a Gaussian distribution. For example, threshold voltages of n-channel devices may be given a range of (0.35, 0.6) Volts (or a mean value of 0.5 V with variance of 0.075 V). Using a range implies the assumption that the threshold voltage (or leakage current, carrier mobility or other parameter) of any n-channel device on the IC will be within the range, with equal probability of being any where in the range. Using the statistical description implies a weighted probability for each device parameter value; most devices are within one standard deviation of the mean. The circuit under testing will be analyzed using the user-selected parameter distribution description and performance parameters modeled based on this description.

Like PARA, PARASTAT will analyze each given design for three different classes of total-dose induced degradation (static degradation, dynamic degradation, and power degradation) for performance predictions. Static degradation occurs when the increased leakage through n-channel devices associated with a signal node is too high for corresponding p-channel devices with decreased current sourcing capabilities to pull that signal node HIGH. Dynamic degradation occurs when the increases in individual delays of each gate when added together to form a path between an input and an output node becomes too high for a synchronous operation. Power degradation occurs when the increased device leakage currents exceeds specification limits determined from the power supply and heat dissipation capabilities. PARASTAT will determine the distribution of total-dose levels associated either with a user-specified amount of degradation or with circuit functional failure for each of these classes of degradation.

C.3 SIMULATOR DESIGN.

PARASTAT uses interval algebra, statistics, switch-level algorithms, and RC-delay estimation techniques to insure fast and efficient simulation with reasonable accuracy. The user-specified type of input, range or statistical, are used to interpret device parameter data. During simulation, the switch-level algorithms will turn a device ON or OFF based on the gate voltage present. Devices are assigned a range of values (or statistical parameters) for resistance chosen from a database of range or statistical parameters derived from the device data. The next gate in the signal path is replaced by a capacitance value chosen in the same manner. This process of converting each and every logic gate into a resistive and capacitive network is carried out until

all gates are covered. Next, degradation calculations for all three mechanisms are carried out for all possible combinations of bias conditions during and after irradiations using RC-delay estimation techniques. The four distinct possible combinations for bias conditions are: (i) LOW during irradiations, LOW-to-HIGH after irradiations, (ii) LOW during irradiations, HIGH-to-LOW after irradiations, (iii) HIGH during irradiations, LOW-to-HIGH after irradiations and (iv) HIGH during irradiations, HIGH-to-LOW after irradiations. After these analyses are completed, PARASTAT results are presented to the circuit designer for verification or analysis.

The mathematical formulae used for degradation estimations are different for the two types of input specifications. For both types, we needed to multiply, add, subtract, and divide two variables with ranges (statistical parameters) at one time or another. Interval algebra mathematics will be used for range data and simple statistical analysis will be used for statistical data. Interval algebra assumes that the given parameter can take any value within the given interval, defined by a minimum value and a maximum value, with equal probability. This interval is also assumed to run over the set of real numbers, R. The following equations present the required operations on two different intervals, (a,b) and (c,d) where a < b and c < d [23].

$$(a,b) + (c,d) = (a+c,\ b+d) \quad (1)$$

$$(a,b) - (c,d) = (a-c,\ b-d) \quad (2)$$

$$(a,b) * (c,d) = (\min(ac,ad,bc,bd),\ \max(ac,ad,bc,bd)) \quad (3)$$

$$(a,b) / (c,d) = (a,b) * (1/c,\ 1/d) \text{ provided } c = 0 \text{ and } d = 0. \quad (4)$$

For statistically varying device parameters, the equations used will be based on the assumptions that each device has device parameters independent of any other device and the distribution of parameters is Gaussian. Also, the functions xy and x/y are approximated to be Gaussian. The assumption of independence is based on the granular nature of the radiation [24]. The required equations, obtained using basic relationships from statistical mathematics [25], are:

assume $x(\mu_X, \sigma_X)$, $y(\mu_Y, \sigma_Y)$, and $z(\mu_Z, \sigma_Z)$

If $z = x + y$, then

$$\mu_Z = \mu_X + \mu_Y$$
$$\sigma_Z^2 = \sigma_X^2 + \sigma_Y^2 \quad (5)$$

If $z = x - y$, then

$$\mu_Z = \mu_X - \mu_Y$$
$$\sigma_Z^2 = \sigma_X^2 + \sigma_Y^2 \quad (6)$$

If $z = xy$, then

$$\mu_Z = \mu_X \mu_Y$$
$$\sigma_Z^2 = \sigma_X^2\mu_Y^2 + \sigma_Y^2\mu_X^2 \quad (7)$$

If $z = x/y$, then

$$\mu_Z = \mu_X/\mu_Y$$
$$\sigma_Z^2 = (\sigma_X^2/\mu_Y^2)+(3\sigma_Y^2(\sigma_X^2+\mu_X^2))/\mu_Y^4 \quad (8)$$

PARASTAT uses the above relationships to obtain final degradation parameters. Based on these degradation parameters, the circuit designer or vendor can easily estimate the proper radiation

tolerance range of DUT. For example, for dynamic failure analysis, one needs to know the delay for each signal path for all four possible input conditions. The RC network obtained by using models for transistors will have a range of values for each of its elements. The total delay for a given signal path is obtained by the sum of the individual delays for each stage. The delay for each stage will be estimated as the product of the pullup (pulldown) resistor value and the output capacitance value. Both of these variables are expected to have range which is used in equation (3) to obtain a range of delay for each individual stage. These delays are added according to equation (1) to obtain a final range for the delay for the signal path under investigation. For processes where statistically varying device parameters are available, equations (7) and (5) are used. Based on these delays, the vendor can easily estimate the reliability (or the confidence level) of a part for dynamic degradation. The same process will be carried out for all degradations to identify the most critical failure mechanism. As the device parameters will be given for various exposure levels, radiation tolerance for each exposure level can be estimated.

PARASTAT can be applied to analysis of a number of circuit designs. The results obtained by running PARASTAT on a full adder circuit have been compared with Monte-Carlo runs on the same circuit using PARA. Figure 68 shows the circuit implementation of the full adder. Figure 69 presents a comparative plot of PARASTAT results and Monte-Carlo results which shows that PARASTAT results compare very favorably with those of Monte-Carlo.

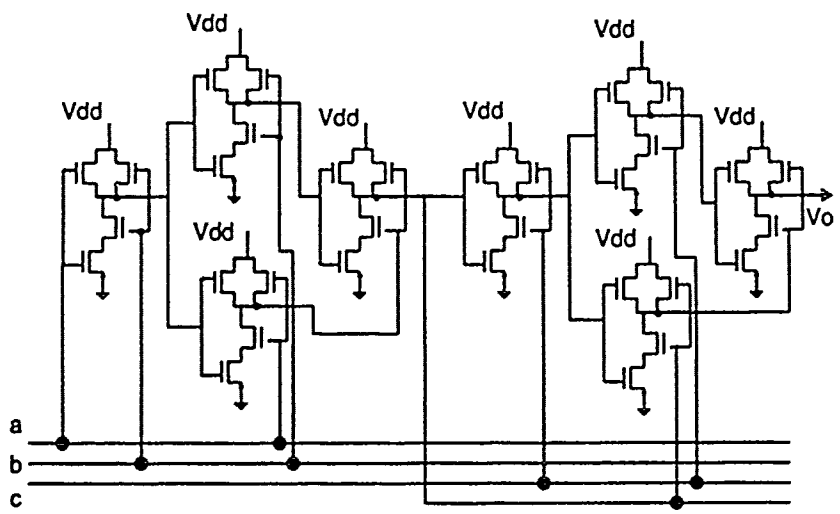

Figure 68. Circuit implementation of the full adder.

C.4 ADVANCEMENT OF STATE-OF-THE-ART.

Parameter variations due to processing and total-dose radiation appear to be independent of one another. Even tight process control of parameter variations does not insure that parameters will maintain these small variations after exposure to ionizing radiation. In fact, circuits designed

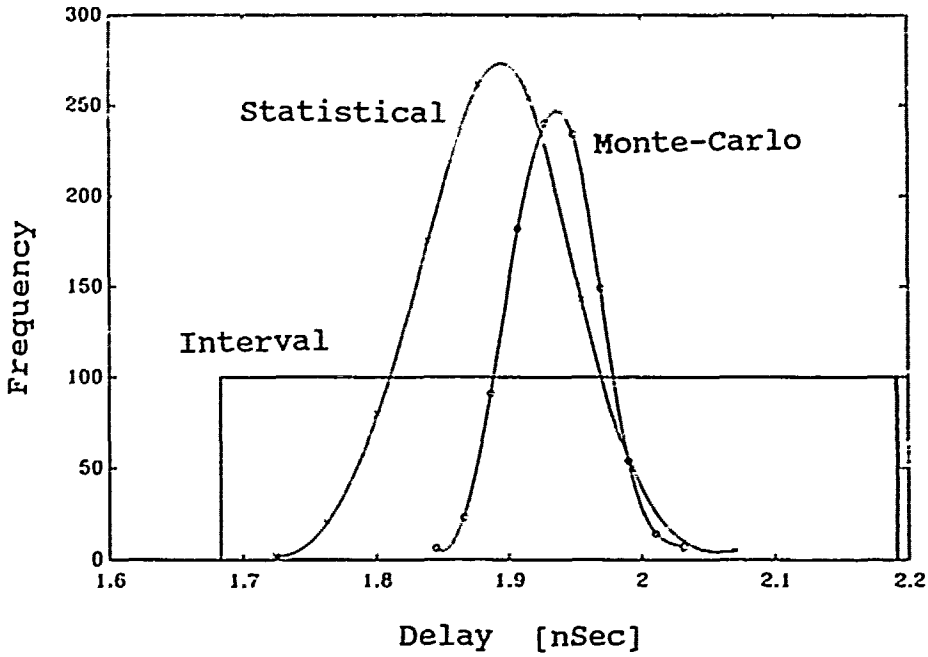

Figure 69. Comparative plot of PARASTAT results and Monte-Carlo results.

with present techniques, which rely on small parameter variations, can be expected to be more sensitive to radiation-induced parameter shifts than their ancestors. Since it is unlikely that the IC manufacturer's reliance on process controls will diminish in the future, simulation codes, such as PARASTAT, which allow for fast, full coverage evaluations of the impact of parameter shifts on functionality and performance, can be expected to become an important adjunct to lot characterization and process characterization measurements for hardness assurance and device qualification.

C.5 STATUS.

We have started working on the code development for PARASTAT. The initial problem has been the conversion of device-level parameters into equivalent resistive models with range of values. These values will be fed to a modified PARA software with statistical analysis capability as described earlier. We anticipate to complete the distributable version of PARASTAT ready within the two years. The software will be made available to all who request it through Vanderbilt University.

APPENDIX D

TODO

D.1 INTRODUCTION.

BiCMOS is an advanced technology in which bipolar and CMOS devices are fabricated on the same substrate, allowing circuit designs with transistor types chosen to optimize subcircuit performance. For example, bipolar devices can be used for current amplification in the output stage, taking advantage of the large current-handling ability of bipolars and enhancing the overall performance of the gate. BiCMOS gates typically include a large amount of CMOS circuitry, thereby reducing their standby power consumption relative to bipolar digital implementations. A simple example of a BICMOS gate is shown in Figure 70 [26].

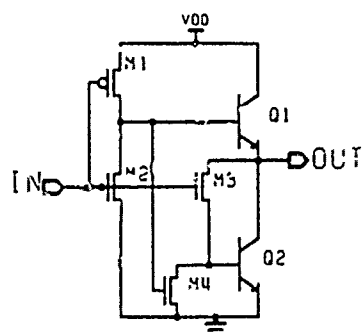

Figure 70. A BiCMOS gate.

The option of combining bipolar and CMOS technologies offers several advantages to designers of radiation-tolerant and radiation-hardened ICs. Since the capacitance present at the output node of a gate for BiCMOS technology can be the same as that of a purely CMOS technology, the increase in current sourcing and sinking capabilities made possible by integrating bipolar devices can decrease the sensitivity of circuit performance to radiation-induced MOS device parameter shifts. Push-pull type bipolar circuits can minimize increases in power requirements for the overall design, while retaining radiation tolerance.

While the future of BiCMOS technology in the radiation effects community is promising, recent advances in BiCMOS design have not been accompanied by the development of computer simulation techniques to model and predict circuit performance and support failure analysis in this new technology. This work introduces a new methodology for simulation of BiCMOS ICs performance levels and failure modes in radiation environments.

D.2 RESPONSE TO RADIATION ENVIRONMENTS.

In MOS integrated circuits, performance degradations associated with radiation exposure are generally attributable to bias-dependent shifts in individual device parameters which in turn cause excessive signal delay or excessive power dissipation in the circuit. The same holds true for BiCMOS technology. The parameters affected by the radiation exposure are threshold voltages, leakage currents, carrier mobilities, and current gains. Since these parameter shifts are bias-dependent, simulation of the impact of radiation on performance or functionality requires thorough coverage of all possible bias conditions for each device and signal path. If conventional device- and circuit-level simulation techniques, such as SPICE, are used, such coverage generally requires prohibitively large amounts of man-hours and computer-power. PARA analyzes the failure modes and levels of CMOS ICs operating in radiation environments [16], translating full SPICE-type device- and circuit-level descriptions of ICs and the parameter shifts associated with their component transistors into a switch-level model and uses this model to determine the failure modes and levels and the worst-case operating conditions of the IC. PARA has been tested on MSI-level CMOS ICs and experiments are currently underway to prove the accuracy of the simulator for LSI and VLSI circuits.

The algorithms used in PARA cannot be applied directly to BiCMOS ICs because switch-level algorithms do not accurately model bipolar devices. Still, the general problem of BiCMOS radiation response simulation has several features in common with the equivalent CMOS problem: the overall performance of BiCMOS ICs depends on bias-dependent shifts for individual devices, and circuit complexity makes SPICE-type modelling at least awkward, if not impossible. New simulation techniques are required for analysis of BiCMOS response to radiation environments.

D.3 SIMULATION ALGORITHMS.

The new simulation approach reported here uses incremental piecewise-linear models for both bipolar and MOS devices. The simulator is called TODO. Like PARA, TODO estimates worst-case bias conditions and predicts the operating performance of ICs exposed to radiation. The input for TODO consists of a SPICE-like circuit description file, and device parameters for MOS and bipolar devices after irradiation for all possible bias conditions.

TODO operates on two different model types, one for each family of transistor. For MOS devices, a resistive model is used. This model approximates each MOS device using a resistor

whose value is determined by the operating conditions during the irradiation and after the irradiation. For example, Figure 71 shows the resistance value curves for an NMOS device, fabricated at MOSIS using their 2.0 μm CMOS process, under various V_{ds} and V_{gs} applied voltages. During circuit simulation, each MOS device is replaced by the equivalent resistor value appropriate to the operating conditions under consideration. Resistor values are chosen from a stored database generated from device data. For bipolar devices, behavior is modelled by replacing the transistor with a current source. The value of the current source is determined from a database generated from the device parameters provided by circuit designers. Figure 72 shows the current values for a bipolar npn device for different values of V_{cc} and I_b.

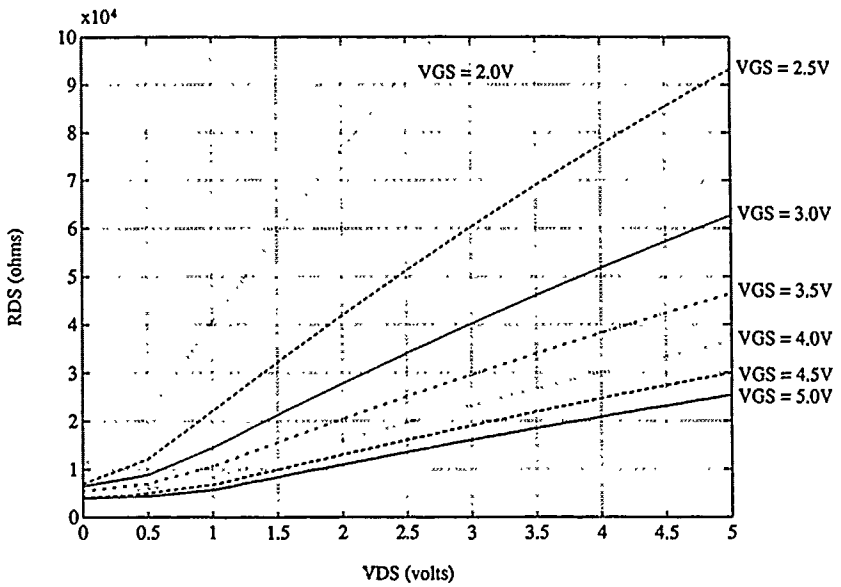

Figure 71. Resistance value curves for an n-channel device.

For the sake of this explanation, assume that nodal voltages at each node in the circuit are known. Using these voltages and topological information, an equivalent circuit is constructed for this set of bias conditions by replacing each MOS device by a resistor and each bipolar device by a current source. Figure 73 shows the TODO model for the circuit shown in Figure 70.

TODO next prompts the user to input his choice of a simulation timestep (we have chosen 0.1 ns for the examples given in this paper). Given this input, TODO calculates the charge flowing into each node in the circuit under the assumption that the device models during one timestep remain constant during one timestep. The final amount of charge present at each node at the end of the timestep is used to calculate the new nodal voltages, and the process is repeated. For example, in Figure 73, the charge being deposited onto node 1 through resistor R_p is obtained by dividing the voltage difference (V_{dd}-V_1) by R_p and then multiplying the result by the timestep. This actually represents the current multiplied by the time to show charge transfer. The same

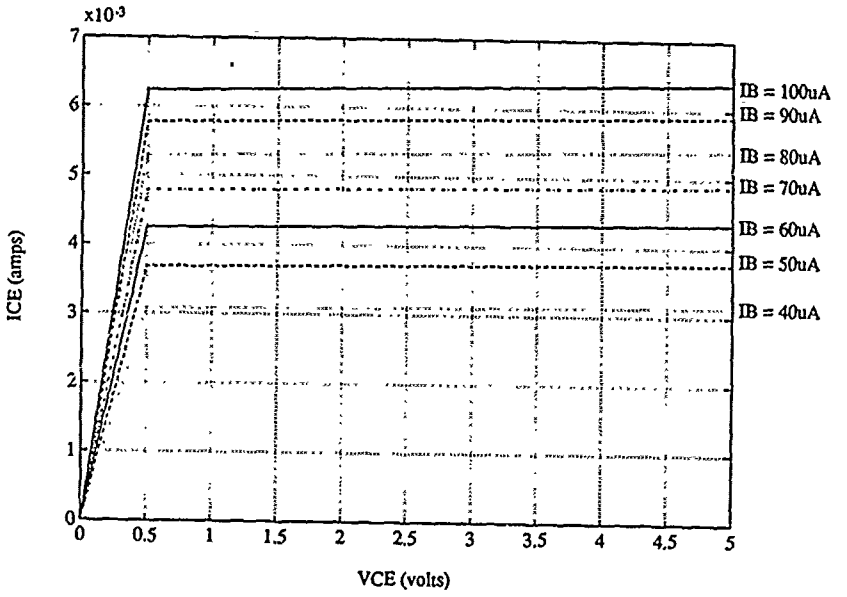

Figure 72. Current values for a bipolar npn device.

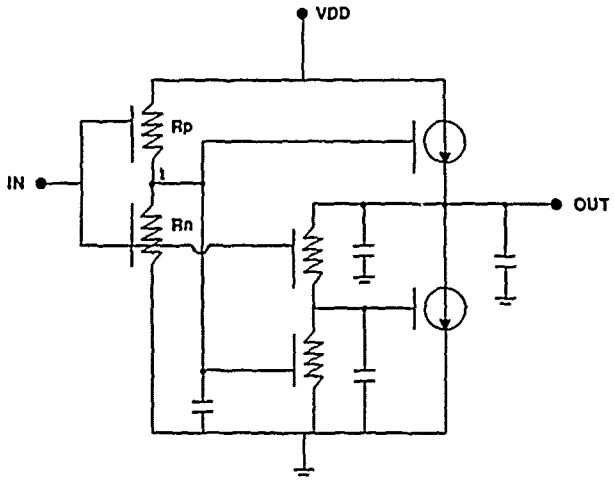

Figure 73. TODO model for the circuit shown in Figure 70.

process is repeated for all the devices associated with a node to obtain the total charge transfer onto the node. For bipolar devices, the charge transfer is integrated to determine the total amount of current passing through the base. This base current value is then used to determine the total current passing through collector and emitter terminals. Using the capacitance value at all nodes, the new voltages at each node are calculated. This computational process is repeated until either a user-input time period has lapsed or the user stops the simulation. At that time all results are

output [27, 28].

Note that these additional algorithms to handle current-driven devices also allow simulation of all-bipolar circuitry, as well as other non-CMOS circuitry, such as NMOS. Thus, TODO extends the PARA capability to cover all modern digital technologies in extensive use.

The inherent limitations associated with similar simulation approaches are the determination of initial conditions for each signal node. For analog circuits, this may cause a great problem, but for digital circuits each signal node in the circuit is either HIGH or LOW reducing the problem to an estimation of worst-case input voltages. TODO initially assigns a consistent set of nodal voltages throughout the circuit and then propagates four signals through the circuit for each input node. These signals are: (i) LOW during irradiation and LOW-to-HIGH after irradiation, (ii) LOW during irradiation and HIGH-to-LOW after irradiation (iii) HIGH during irradiation and LOW-to-HIGH after irradiation and (iv) HIGH during irradiation and HIGH-to-LOW after irradiation.

These signals are assumed to invert at each stage. The results of the signal propagation for all these cases are automatically examined later by TODO and the worst-case bias conditions and critical subcircuits associated with failure are identified. The circuit designer then has the option to modify the element causing the failure or redesign the circuit based on the knowledge of the failure.

D.4 ADVANCEMENT OF THE STATE-OF-THE-ART.

Simulation tools, such as TODO, will become increasingly important as the device densities of ICs continue to increase. Conventional circuit simulators are not capable of modelling even MSI-level circuit responses to radiation environments because such simulations require computationally demanding coverage of multiple bias-condition-dependent device parameters for each component transistor. Simulators such as TODO make such analyses possible and therefore are necessary as support to radiation-tolerant and radiation-hardened circuit design.

D.5 STATUS.

The initial version of TODO to verify the accuracy and validity of the algorithms has been completed. However, due to the emphasis on validation and not on efficiency, the software package is not fully distributable. As we can not offer software support, we have decided not to distribute software which are only developed for demonstration purposes or for validation purposes. We also do not have any funding currently to develop a distributable version of TODO for radiation effects community. We will develop an efficient and distributable version of TODO in the future whenever time and funds permit us.

APPENDIX E

SIMULATION OF TRANSIENT RADIATION EFFECTS ON CMOS ICS

E.1 INTRODUCTION.

The effects of transient, pulsed radiation on the operation of integrated circuits (ICs) has been of critical concern to the circuit designers of the radiation-effects community. The charges generated as a result of such exposure either recombine with each other or are collected as well or substrate currents [29]. These currents may attain values high enough to cause resistive-rail-span-collapse (RRSC) phenomena. RRSC has been shown to be the dominant mechanism for operational failure of ICs in transient radiation environments [30]. Under RRSC, the currents collected by well and substrate contacts, which are connected to the power lines, have large magnitudes and may drop a significant p..centage of available supply voltage due to the resistance offered by the power distribution network. This drop in the supply rails may be large enough to cause malfunctioning of ICs during irradiation. Due to high reliability requirements associated with the ICs operating in dose-rate environments, thorough simulation is necessary to verify the radiation tolerance of circuit designs against RRSC.

For simulation of RRSC, each charge collecting node in the circuit can be replaced by a current source and the power distribution network can be replaced by a resistive network. This will yield a network of passive elements which can be solved easily by many of the known simulation techniques. If the magnitudes of the current passi g through each branch of the power distribution network are known, the circuit designer can change the resistance offered by the network to reduce the risk of operational failure. Accurate predictive modeling of such phenomena is required during the design stages to aid the designer to achieve optimum radiation failure-exposure levels. However, the such predictions are computationally intensive and require long man-hours to generate accurate models.

The problems arising from the computational complexity inherent in the dose-rate simulations have been solved for the case of regular arrayed structures, such as memory ICs [31]. For such ICs, analyses is first carried out on an individual memory cell to determine the well and substrate currents for that cell. Assuming that each cell in the IC operates independently and collects charges during irradiation independently, it is clear that the well and substrate currents for each cell will be identical. For simulations, each memory cell is replaced by a current source whose value is equal to the estimated well current and each power bus segment is replaced by its resistance. This will yield a passive network of resistances and current sources which can easily be solved. Because of the uniform nature of the radiation, the identicity of memory cells is a very reasonable assumption.

However, for combinational circuits, the identicity assumption for all individual cells does not hold true. Usually, for a combinational circuit, all wells on an IC are of different size and shape.

Another factor affecting the modeling is the total number of well contacts per well. If the number of well contacts in the well is more than one, the amount of charge collected by each well contact will be dependent on the well shape and the position of the well contacts. RRSC phenomena further will depend on the power bus structure within the cell and outside the cell. Also, for these simulations, the extraction of power distribution network in terms of current sources and resistances requires long man-hours and tedious, repetitive tracing technique. An automated system for such an analyses will enhance the circuit designer's capabilities for achieving optimum radiation tolerance.

Mavis et al. have proposed an approach consisting of a semi-automated analysis technique using hierarchical macrocell modelling [32]. In their approach, each sub-cell as designed by the circuit designer is analyzed separately to obtain its specific equivalent circuit. This process is carried out for all cells and the results are combined to produce a chip-level description for final analysis. Their approach seems to assume that each sub-cell collects charges from transient radiation independently of all sub-cells around it. This assumption holds when the sub-circuit do not share a common well or when they do not abut. However, in combinational circuits, two abutting cells may have their well touching each other to reduce spacing requirements. For example, for standard CMOS non-hardened MOSIS process, the distance between two non-overlapping wells is required to be 6λ. Instead, if these well are abutting each other, only the regions inside the well needs to be adequately separated. The largest required distance inside a well is the distance between two active regions which is only 3λ. Thus a saving of space is easily achieved by having a uniform well stretching across various cells. For such designs, the individualized analysis of each cell may overpredict the current during a dose-rate event. This overestimation of generated current will result in underestimations of the dose-rate upset level.

To overcome all of the problems mentioned above, a new simulation approach is necessary. We have broken down our simulation methodology into four different tasks; current estimation, power distribution network extraction, actual simulation, post-simulation interface. Figure 74 shows the flowchart of the whole simulation process. For accurate current estimation for (or charge collected by) each well-contact in a layout, we will use a geometrical technique for the automated extraction and assignment of the photocurrent components. For power distribution network extraction, a pixel-plane based approach with scan-line algorithm will be used. For circuit simulation, we will use SPICE and RSIM. The post-simulation interface will enable the circuit designer to identify the critical parts of the power network directly on the layout. All of these tasks are described in the following sections.

E.2 WELL PARTITIONING TECHNIQUES.

The proposed current estimation algorithm uses a simple geometric technique on entire well to divide it into components for each well contact within that particular well. Each well contact is assumed to collect all the charges generated in its assigned portion of well. This means if a well has only one contact, the entire well is assigned to that contact. If a well has more than one contact, say n contacts, then that well is divided into n parts and each contact assigned one of

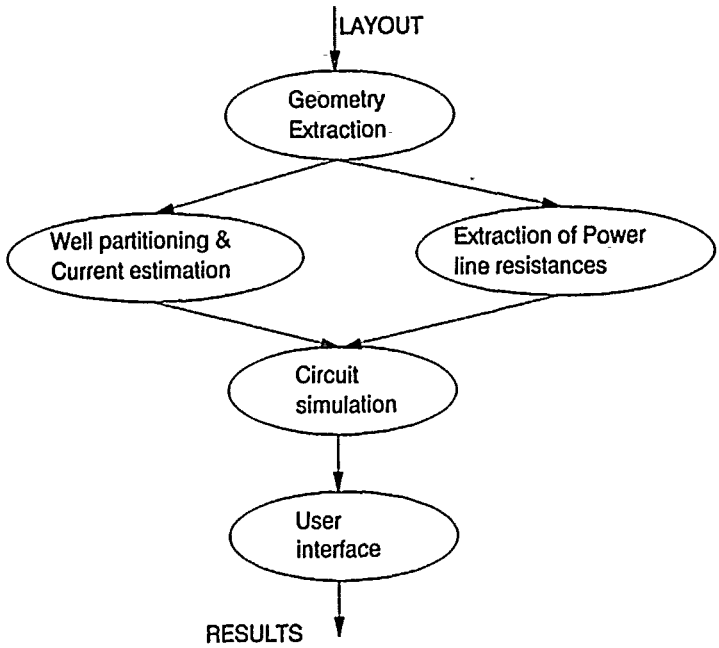

Figure 74. Flowchart for the simulation process.

the parts. The portion of the well assigned to each contact is determined from the position of all the well contacts, shape of the well, and the size of the well. The well division is based on the assumption that the charges generated in the well area will be collected by the nearest contact. For example, for the well shown in Figure 75, the left contact will collect all the charges generated in the left 1/3rd of the well. While all charges generated in the right 2/3rds of the well will be collected by the right contact. This partitioning will ensure that all the charges in the well will be collected by the nearest contact. This partitioning routine assumes uniform charge generation throughout the well area.

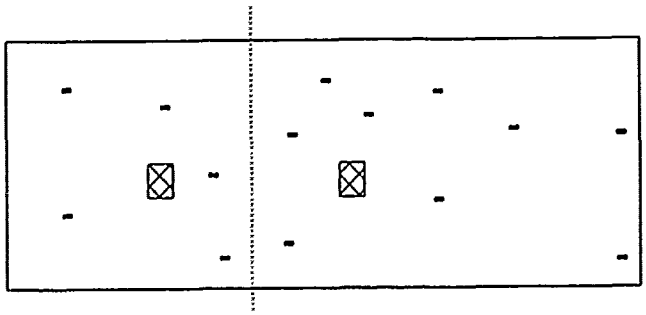

Figure 75. The left contact will collect 1/3rd of the total charge while rest will be collected by right contact.

The simple algorithm used for the partitioning of the well connects the contact under consideration with another contact and bisects the line joining these two contacts. This bisecting line is extended until it meets the boundary of the well or another bisecting line. This process is repeated for all contacts in a well. A pseudocode for this routine is as follows:

```
For (each well contact)
        {
        Draw lines joining all other contacts to this contact;
        Bisect each of these lines one by one;
        Extend the bisecting line until
                {
                another bisecting line is reached;
                OR
                well boundary is reached
                }
        }
```

Figure 76 shows an irregularly shaped well with several well contacts and extended bisecting lines for these well contacts.

Once the well has been partitioned, the estimation of current passing through each contact can easily be calculated by using modified Wirth-Rogers [33] equations. These currents then can be used along with extraction algorithms to generate an input file for any conventional simulator.

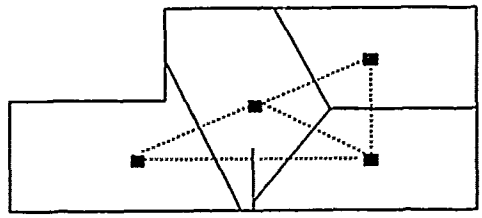

Figure 76. An irregular shaped well with partitioning and bisecting lines.

The actual partitioning algorithm accepts a layout file in the CIF format. This CIF file is first flattened and the total chip area estimated from the top most cell. Based on this size, a pixel-plane is created [34]. In this pixel-plane, each pixel represents one square μm of the layout surface. Each of these pixel contains information about the various layers present at that particular square μm. For our routines, we have assigned one eight-bit number to each pixel with each bit representing the presence or absence of a layer. For example, metal1 layer was assigned bit 0. From the CIF file, each metal1 box is mapped on the pixel-plane by ORing the first bit of each pixel which would fall under the box with 1. Entire chip is mapped onto the pixel-plane in this fashion. This technique will allow easy tracing capabilities for metal wires and resistance extraction and also speeds up the well partitioning algorithms.

The actual well partitioning algorithms work as follows on the pixel-plane. First of all, a vertical scan line is passed across the pixel-plane [33]. Here vertical means all pixels in a vertical line fall on the scan line. During scanning, all these pixels are inspected for the presence or absence of certain layers. Whenever the scan line encounters a pixel which has the well bit set to 1, it goes back to check the previous scan line position to see if the pixel in the same vertical position on that line also contained a well. If it did, the new pixel is considered as part of the well and scanning process is continued. If the previous scan line pixel did not have the well bit set, the routine assumes that a new well is found and proceeds accordingly. The problem with such algorithms is the connectivity of wells. For example, for the well shown in Figure 77, the scan line will assume that there are two different wells as it starts scanning from left to right. After the scan has reached the line AA', it becomes clear that those wells are connected. For such cases, we have made provisions to make sure that all such wells get connected at the end of a scan. During this scanning, all well contacts are also extracted along with the associated wells. As only bitwise logic operations are required, the scanning process is fast and efficient.

Next, the partitioning algorithm is run on this extracted data. The extracted data contains the information regarding well shape and size and the contacts within each well. The well partitioning for each of these well contacts is done serially. First of all a well contact is picked randomly and the whole well area is assigned to it. Next another contact is picked and a bisection of the well is performed between these two contacts and a portion assigned to the contact under consideration. Next, another contact is picked and the same process of partitioning is carried out. During all these partitioning processes only reduction in the previously assigned areas is considered, i.e., if the new partition adds more area to the partition assigned from the previous bisection routine, the new partition is ignored. The same process is repeated for all contacts. Finally, the well perimeter area is calculated for all contacts from its assigned partition. For all these contacts, their perimeter line is extended by one diffusion length to accommodate the diffusing carriers.

To prove the validity of the partitioning algorithm, we designed an IC using 2.0 μm, nwell, non-hardened, MOSIS CMOS process. Figure 78 shows the entire chip with all different shapes and sizes of wells with varying number of contacts per well. This IC was irradiated under continuous laser beam of 2.0 mW power. The well and substrate contacts were biased at 5V. The resulting currents coming out of well contacts was measured by HP7405B parameter measurement system.

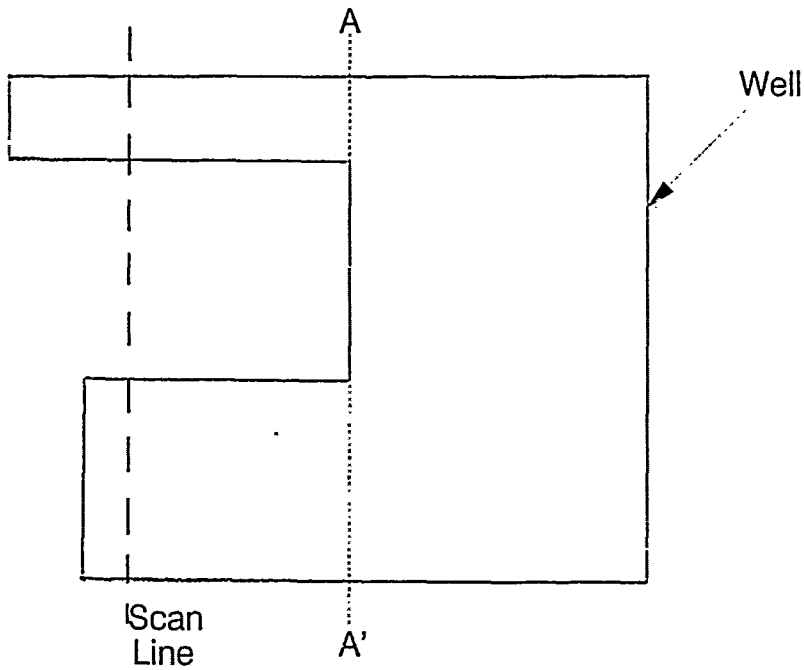

Figure 77. The scan line will see two different well initially eventhough only one well exists.

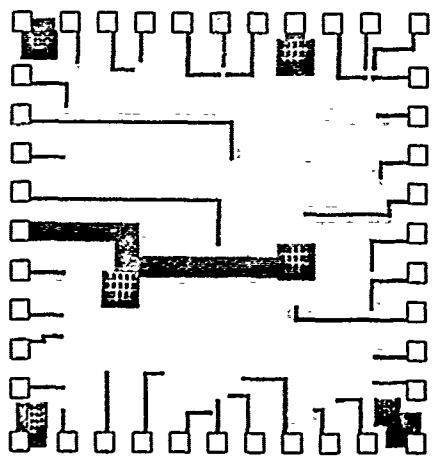

Figure 78. The IC design used for the experiment.

We irradiated various wells with the results shown in Table 14 along with the shape and size of the well. As expected from the theoretical discussion before, the well shown in (a) had the current evenly divided between the two contacts. This is because of the symmetrical placement of the contacts with respect to the well. The partitioning algorithm also proved the same. Table 14 shows only a small number of well shapes which were interesting from the partitioning point of view. For different shapes and sizes of wells, as shown in the table, the partitioning algorithm correctly estimated the division of the well current between contacts in a well. This clearly shows that the assumption that the charges will be collected by the nearest well contact is true for this fabrication process. This will also hold true for all technologies and fabrication processes. With higher doping densities (smaller line widths), only the number of charges generated in the substrate and well will be different. Also, the diffusion length by which the well perimeter needs to be extended will be different. However, the partitioning algorithm will not be affected by any of these and will still provide accurate estimation for charge collection.

Table 14. Results of the experiment and software analysis.

Well Shape	Current Partitioning	
	Theoretical	Experimental
	1 : 1	1 : 1.01
	1 : 1 : 1.43	1 : 0.94 : 1.51
	1 : 1.31	1 : 1.41
	1 : 1.56 : 1.71	1 : 1.38 : 1.53
	1 : 1.94	1 : 2.06

The identification of contacts and partitioning of wells is done by scan-line algorithm which guarantees a constant computation time for the same size IC. The number of contacts per well may affect the computation time by a small amount, but the overall computation complexity will only be a function of the size of the IC.

E.3 RESISTANCE EXTRACTION.

For the simulation of RSCC, one needs the resistive values of the power line segments. With the IC mapped to the pixel-plane, the extraction of these resistive elements reduces to just another scan of the pixel-plane. However, a simple scan as performed in the case of well extraction will not work due to the directionality of the resistance values (depending on the direction of the current flow, the resistance of a rectangular box will change). One must first establish the direction of the current flow in the power network and then extract the resistance values.

To obtain the current flow direction, the power network is first broken down into the minimal size boxes, i.e., all boxes present on metal1 and metal2 are broken down into smallest rectangle possible. Each of these rectangles have pointers pointing to its four neighbors on each side and a pointer for the side through which the current is expected to enter the rectangle. This process of breaking down in performed by scanning the pixel-plane in much the same way as described above. Also, a box is broken down whenever a well contact is encountered. Figure 79a shows a section of the power line and Figure 79b shows the same section after it has been broken down into minimal size boxes.

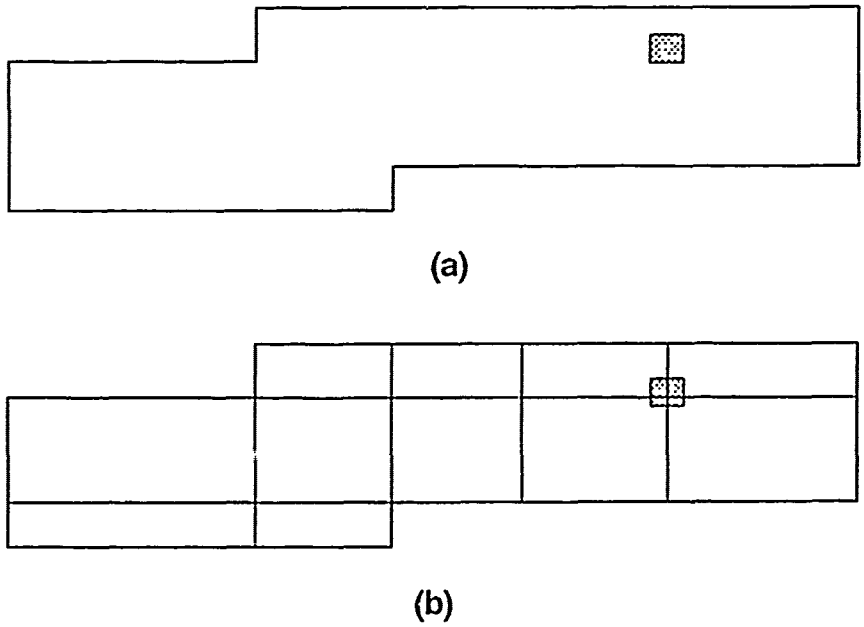

Figure 79. The breaking down of power line into minimal size tiles.

Next, the location of the Vdd pad is obtained from the designer and the power network is traced through these minimal size boxes. The current is expected to flow from the Vdd pad into the boxes adjacent to it through the common side. These same boxes are then used to identify the current flow direction for their neighbors. This process is repeated for all the boxes using a depth first search algorithm. At the end of this search, we will have all metal boxes with the current flow indicator set in the right direction.

Next, all these boxes are converted into resistances one by one and the resultant input file for simulation prepared for the final simulation. The node names for resistances for each of the box are given as the lower lefthand corner X_Y, i.e., if the lower left hand corner coordinates for box1 are (25,1280) and the same for its neighbor box2 is (35,1290), then the resistance of box1 will be given node numbers 25_1280 and 35_1290. This type of numbering system allows for easy identification of the critical boxes after simulation. However, some simulators, such as SPICE2G6, do not accept the node names with non-numeric characters. For those type of simulators, we have created an interface which will convert these node names into numeric numbers and keep track of all the boxes. The node numbers for the current sources for the well contacts is obtained in the similar way by using the lower leftmost coordinates of the well contact.

E.4 SIMULATION.

The final file for simulation is created with all the current sources and all the resistance values. The circuit simulation is carried out on these files to obtain the power rails for all the circuit. We have developed a simulator, RSIM, based on the conjugate gradient method for DC analysis of passive elements. RSIM simulates the distributed power supply voltages and currents, and the resulting noise margins. A unique and compact circuit description language has been used in RSIM to reduce the overhead associated with conventional circuit simulators. Also, speed improvements are achieved through modular storage structure and advanced numerical algorithms specifically suited for the dose-rate effects analysis. RSIM has been tested on several circuits for the analysis of power supply noise margins. The accuracy of the simulation has been verified by independent simulations on conventional circuit simulators. RSIM outputs the nodal voltages of each and every node in the power distribution network. The output of RSIM is fed into the post-processor routines for interfacing with the circuit designers.

This post-processor routine is capable of detecting the critical power rails in a given design. This routine goes through the simulation results obtained from the circuit simulator, say RSIM, and assigns each node of the power network into one of the ten intervals from GND to Vdd depending on the node voltage. These nodes are then converted back into original CIF boxes and a new layout file is generated. This file will contain only the power distribution network showing the rail span of the whole circuit with different intervals assigned different colors on the screen. These resultant files can be used to identify the critical boxes on the layout.

E.5 RESULTS.

The above software was run on several circuits. One of the ICs was a 4-bit multiplier using parallel multiplication algorithm. Another design was a programmable clock generator. A third design was an 8-bit parallel multiplier. All of these ICs were manufactured by MOSIS using their non-hardened, 2.0 μm, CMOS, n-well process. In all the cases, the simulator identified the critical sub-sections of the power network which would have caused failure.

The one main drawback of the software program has been the memory requirements due to pixelplane algorithms. The above mentioned ICs are 2.5mm X 2.5mm in size. The memory requirements for such an IC are in the 10Mbit range. For larger ICs, better memory management is required. We plan to use paging and divide-and-conquer techniques to reduce memory requirements in the next version.

E.6 STATUS

The above described software has been implemented on UNIX system in "C" programming language. The initial version of the software is extremely slow and was intended to demonstrate the feasibility of the project. We are currently intending to improve the algorithms and software efficiency by using innovative programming techniques. The second version of the software will not be finished for a long time due to unavailability of funds for this project. If funds are available, the improvements in the software will be implemented and the latest version made publicly available to radiation effects community.

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